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# Centauri

ATX

Ver:A00

## CPU:

INTEL HSW-E LGA2011-3

## System Chipset:

INTEL - Wellsbug

## OnBoard Chipset:

HD Audio Codec:Creative Malcolm

LAN-Killer E2205 x1

eSIO: NCT6683D-T

Flash ROM: 64 Mb SPI Quad Read

## Main Memory:

DDR4 (2133MHz) \* 4 (Qual Channel) @1.2V

## Expansion Slots:

PCI Express (X16) Slot \* 3


PCIe(X1) Slot \* 1

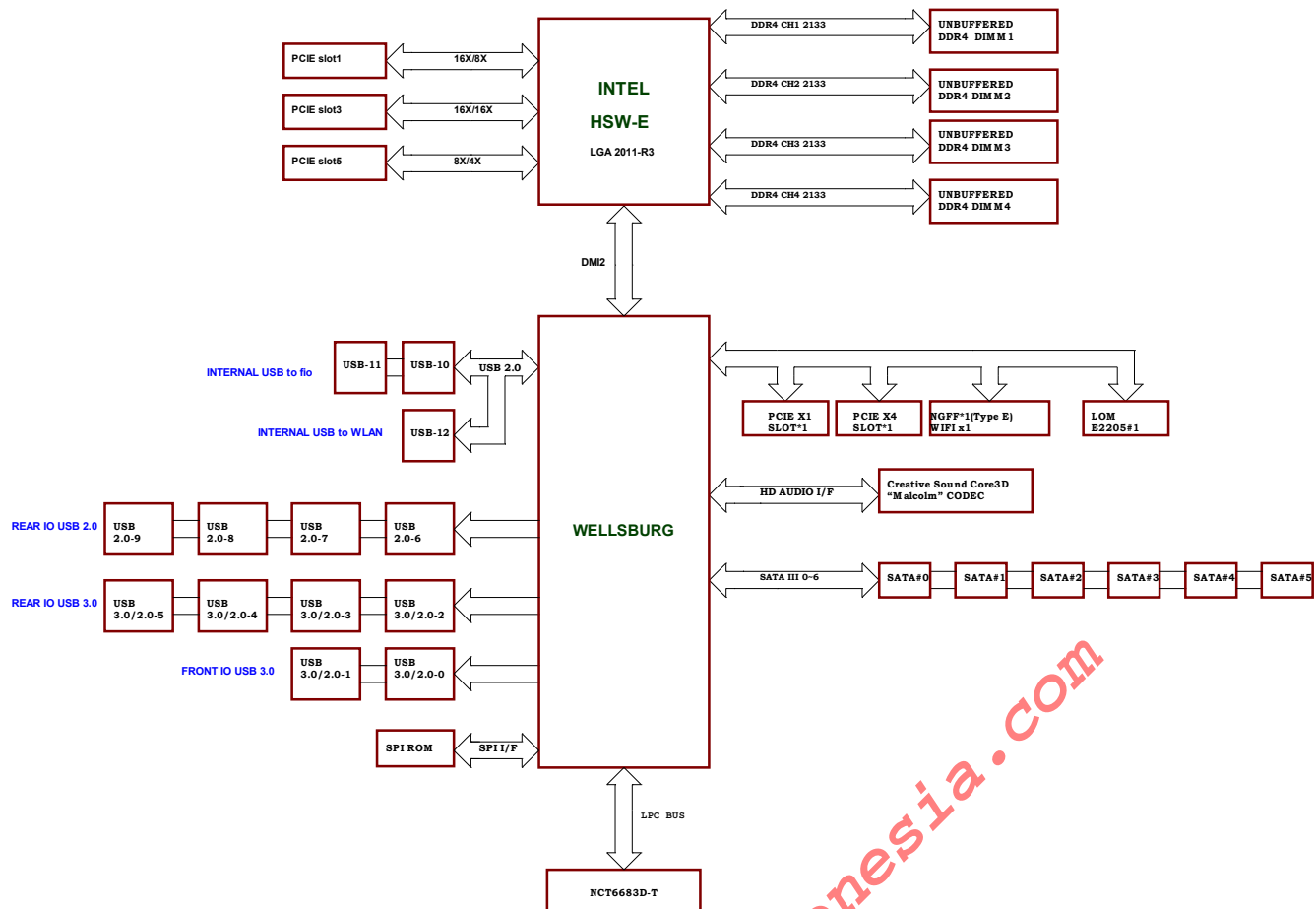
PCIe(X4) Slot \* 1

NGFF\_S1(WLAN) \* 1

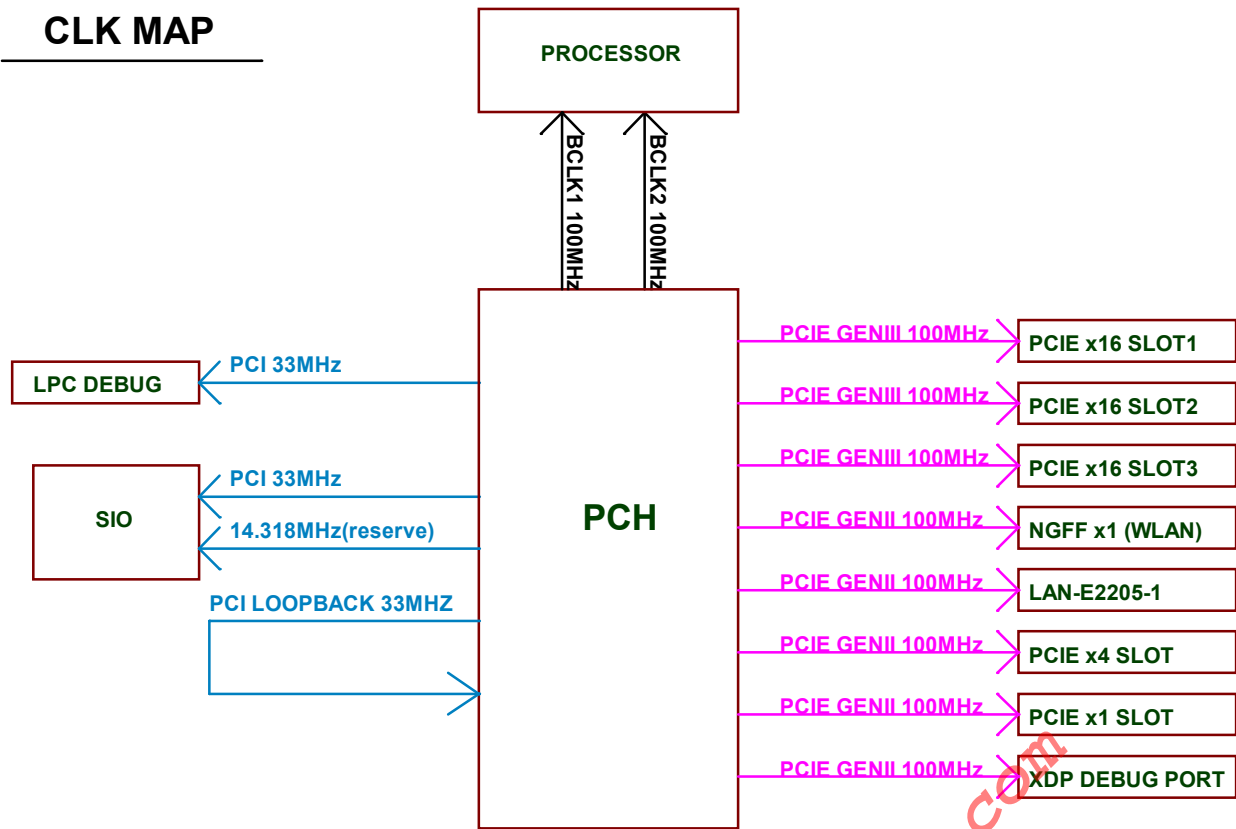
## PWM:

VRD12.5 - ISL6376 Extend to10-Phase Dr.MOS

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# CLK MAP



## G3-->S5-->S0

3VSB

PCH\_DPWROK

RSMRST#

PSIN#

PWRBTN#

SLP\_S5#

SLP\_S4#

SLP\_S3#

PS\_ON#

+12V/VCC5/VCC3

WBG\_1P05

CPU\_IO

PCH\_1P5\_PLL

VPP\_2P5V

VCC\_DDR

VCCP

VRM\_PGD

MEM\_PWRGD

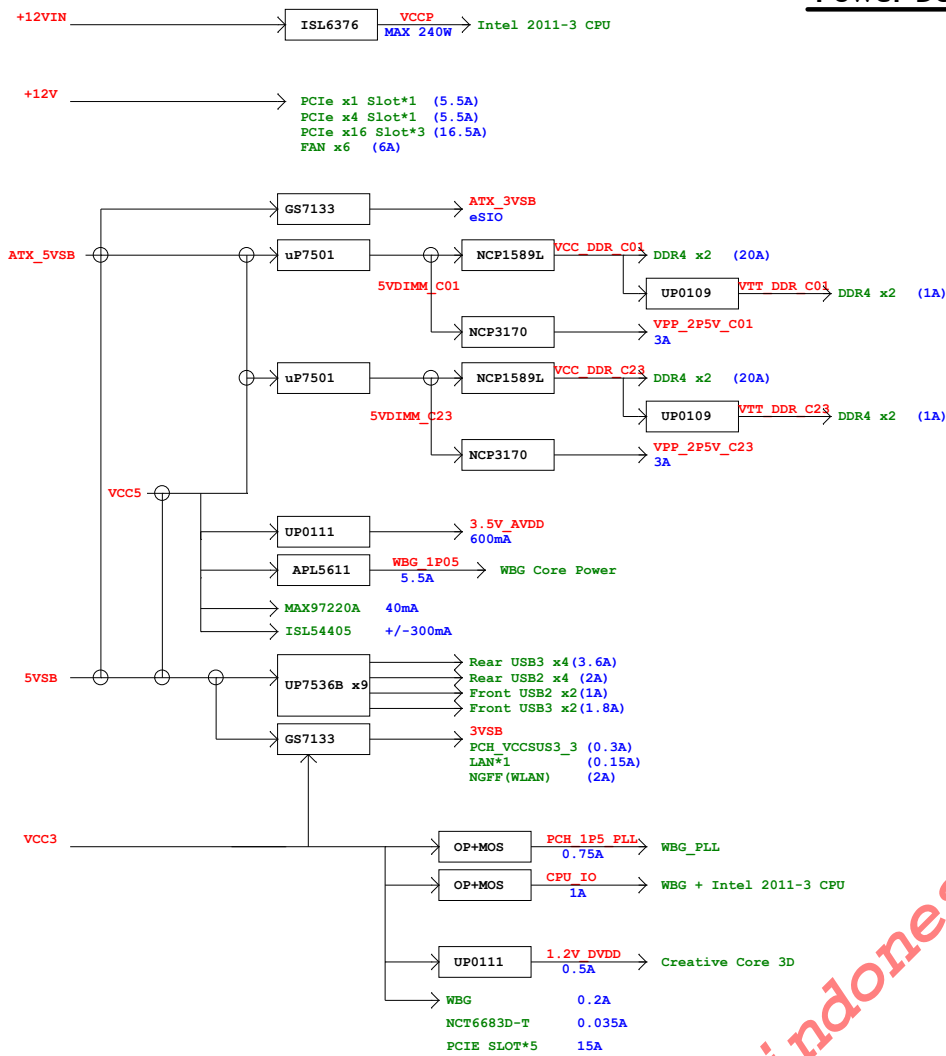
H\_PWRGD

PWRGD\_3V

PLTRST#

PLTRST\_CPU#

## Power Delivery



MSI Micro-Start Intl Co., Ltd.		
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15 MEM\_MA\_DATA[63..0] ← MEM\_MA\_DATA[63..0]

CPU1B

HASWELL-E

MEM\_MA\_DATA63 CK38  
MEM\_MA\_DATA62 CM38  
MEM\_MA\_DATA61 CK34  
MEM\_MA\_DATA60 CM34  
MEM\_MA\_DATA59 C139  
MEM\_MA\_DATA58 CL39  
MEM\_MA\_DATA57 CM35  
MEM\_MA\_DATA56 CL35  
MEM\_MA\_DATA55 CD38  
MEM\_MA\_DATA54 CF38  
MEM\_MA\_DATA53 CD34  
MEM\_MA\_DATA52 CF34  
MEM\_MA\_DATA51 CC39  
MEM\_MA\_DATA50 CM39  
MEM\_MA\_DATA49 CC35  
MEM\_MA\_DATA48 CE35  
MEM\_MA\_DATA47 CC31  
MEM\_MA\_DATA46 CE31  
MEM\_MA\_DATA45 CC27  
MEM\_MA\_DATA44 CE27  
MEM\_MA\_DATA43 CB32  
MEM\_MA\_DATA42 CD32  
MEM\_MA\_DATA41 CB28  
MEM\_MA\_DATA40 CD28  
MEM\_MA\_DATA39 C131  
MEM\_MA\_DATA38 CL31  
MEM\_MA\_DATA37 CJ27  
MEM\_MA\_DATA36 CH27  
MEM\_MA\_DATA35 CH32  
MEM\_MA\_DATA34 CK32  
MEM\_MA\_DATA33 CM32  
MEM\_MA\_DATA32 CH28  
MEM\_MA\_DATA31 CL13  
MEM\_MA\_DATA30 CM12  
MEM\_MA\_DATA29 CD14  
MEM\_MA\_DATA28 CC14  
MEM\_MA\_DATA27 CH14  
MEM\_MA\_DATA26 CM14  
MEM\_MA\_DATA25 CG15  
MEM\_MA\_DATA24 CE13  
MEM\_MA\_DATA23 CB9  
MEM\_MA\_DATA22 CK8  
MEM\_MA\_DATA21 CE11  
MEM\_MA\_DATA20 CD10  
MEM\_MA\_DATA19 C111  
MEM\_MA\_DATA18 CK10  
MEM\_MA\_DATA17 CF8  
MEM\_MA\_DATA16 CE9  
MEM\_MA\_DATA15 BY12  
MEM\_MA\_DATA14 CA11  
MEM\_MA\_DATA13 BU15  
MEM\_MA\_DATA12 BY14  
MEM\_MA\_DATA11 BY14  
MEM\_MA\_DATA10 BW13  
MEM\_MA\_DATA9 BU11  
MEM\_MA\_DATA8 BY12  
MEM\_MA\_DATA7 CB8  
MEM\_MA\_DATA6 CA7  
MEM\_MA\_DATA5 BU9  
MEM\_MA\_DATA4 BT8  
MEM\_MA\_DATA3 CB8  
MEM\_MA\_DATA2 CA9  
MEM\_MA\_DATA1 BT8  
MEM\_MA\_DATA0 BU7

CR11  
CP10  
CN9  
CU11  
CW11  
CV8  
CX8  
CY8  
CZ8  
DDRO\_CLK\_DP[3]  
DDRO\_CLK\_DP[2]  
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DDRO\_CLK\_DP[0]  
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DDRO\_CLK\_DN[1]  
DDRO\_CLK\_DN[0]  
DDRO\_BG[1]  
DDRO\_BG[0]  
DDRO\_BA[1]  
DDRO\_BA[0]

DDRO\_DQS\_DP[17]  
DDRO\_DQS\_DP[16]  
DDRO\_DQS\_DP[15]  
DDRO\_DQS\_DP[14]  
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DDRO\_DQS\_DP[2]  
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DDRO\_DQS\_DP[0]  
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DDRO\_DQS\_DN[16]  
DDRO\_DQS\_DN[15]  
DDRO\_DQS\_DN[14]  
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DDRO\_MA[6]  
DDRO\_MA[5]  
DDRO\_MA[4]  
DDRO\_MA[3]  
DDRO\_MA[2]  
DDRO\_MA[1]  
DDRO\_MA[0]  
DDRO\_CKE[5]  
DDRO\_CKE[4]  
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DDRO\_CS\_N[0]  
DDRO\_CID[2]  
DDRO\_ACT\_N  
DDRO\_ALERT\_N  
DDRO\_PAR

CU9  
CM36  
CF36  
CE29  
CL29  
CG14  
CG8  
BU13  
BV8  
CV10  
CZ7  
CC37  
CD30  
CK30  
CK14  
CH10  
BV12  
BU6  
CW9  
CK36  
CD36  
CG29  
CF29  
CH8  
BV14  
BW8  
CT10  
CL37  
CE37  
CM30  
CJ13  
CG11  
BW11  
BV6  
CD24  
CL23  
CL25  
CJ21  
CE23  
CF17  
CE18  
CF24  
CK18  
CJ19  
CH18  
CN19  
CL19  
CZ20  
CN21  
CT22  
CZ21  
CP22  
CC15  
CN15  
CC12  
CF16  
CE17  
CJ17  
CE25  
CF24  
CC24  
CJ23  
CN25  
CF22  
CK28  
CK24  
CD28  
CH29  
CJ24  
CK24  
CC25  
CF28  
CH22  
CD22  
CJ25  
CK46  
CD16  
CK20

MEM\_MA\_DQS\_H7 15  
MEM\_MA\_DQS\_H6 15  
MEM\_MA\_DQS\_H4 15  
MEM\_MA\_DQS\_H3 15  
MEM\_MA\_DQS\_H2 15  
MEM\_MA\_DQS\_H1 15  
MEM\_MA\_DQS\_H0 15  
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MEM\_MA\_DQS\_L6 15  
MEM\_MA\_DQS\_L5 15  
MEM\_MA\_DQS\_L4 15  
MEM\_MA\_DQS\_L3 15  
MEM\_MA\_DQS\_L2 15  
MEM\_MA\_DQS\_L1 15  
MEM\_MA\_DQS\_L0 15  
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MEM\_MA\_ADD16 15  
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MEM\_MA\_ADD14 15  
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MEM\_MA\_ADD11 15  
MEM\_MA\_ADD10 15  
MEM\_MA\_ADD9 15  
MEM\_MA\_ADD8 15  
MEM\_MA\_ADD7 15  
MEM\_MA\_ADD6 15  
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MEM\_MA\_ADD4 15  
MEM\_MA\_ADD3 15  
MEM\_MA\_ADD2 15  
MEM\_MA\_ADD1 15  
MEM\_MA\_ADD0 15  
MEM\_MA\_CKE1 15  
MEM\_MA\_CKE0 15  
MEM\_MA\_ODT1 15  
MEM\_MA\_ODT0 15  
MEM\_MA\_CS0 15  
MEM\_MA\_CS1 15  
MEM\_MA\_CS2 15  
MEM\_MA\_CS3 15  
MEM\_MA\_C2 15  
MEM\_MA\_ACT# 15  
MEM\_MA\_ALERT# 15  
MEM\_MA\_PAR 15

MEM\_MA\_ADD[17..0] ← MEM\_MA\_ADD[17..0] 15

15 MEM\_MA\_CLK2\_H  
15 MEM\_MA\_CLK0\_H  
15 MEM\_MA\_CLK2\_L  
15 MEM\_MA\_CLK0\_L  
15 MEM\_MA\_BG1  
15 MEM\_MA\_BG0  
15 MEM\_MA\_BA1  
15 MEM\_MA\_BA0

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16 MEM\_MB\_DATA[63..0] ← MEM\_MB\_DATA[63..0]

CPUIC

### HASWELL-E

MEM_MB_DATA63	DE39	DDR1_DQ[63]	DDR1_DQS_DP[17]	CW13
MEM_MB_DATA62	DF38	DDR1_DQ[62]	DDR1_DQS_DP[16]	DD36
MEM_MB_DATA61	DB36	DDR1_DQ[61]	DDR1_DQS_DP[15]	CV36
MEM_MB_DATA60	DC35	DDR1_DQ[60]	DDR1_DQS_DP[14]	DA31
MEM_MB_DATA59	DA39	DDR1_DQ[59]	DDR1_DQS_DP[13]	CU23
MEM_MB_DATA58	DC39	DDR1_DQ[58]	DDR1_DQS_DP[12]	DC7
MEM_MB_DATA57	DF36	DDR1_DQ[57]	DDR1_DQS_DP[11]	CW3
MEM_MB_DATA56	DC37	DDR1_DQ[56]	DDR1_DQS_DP[10]	CH4
MEM_MB_DATA55	CT38	DDR1_DQ[55]	DDR1_DQS_DP[9]	BV2
MEM_MB_DATA54	CV38	DDR1_DQ[54]	DDR1_DQS_DP[8]	DB14
MEM_MB_DATA53	CT34	DDR1_DQ[53]	DDR1_DQS_DP[7]	DB38
MEM_MB_DATA52	CV34	DDR1_DQ[52]	DDR1_DQS_DP[6]	CR37
MEM_MB_DATA51	CR39	DDR1_DQ[51]	DDR1_DQS_DP[5]	DD32
MEM_MB_DATA50	CU39	DDR1_DQ[50]	DDR1_DQS_DP[4]	CT30
MEM_MB_DATA49	CR35	DDR1_DQ[49]	DDR1_DQS_DP[3]	DB10
MEM_MB_DATA48	CU35	DDR1_DQ[48]	DDR1_DQS_DP[2]	CT4
MEM_MB_DATA47	DE33	DDR1_DQ[47]	DDR1_DQS_DP[1]	CJ5
MEM_MB_DATA46	DA33	DDR1_DQ[46]	DDR1_DQS_DP[0]	BY4
MEM_MB_DATA45	CY28	DDR1_DQ[45]		
MEM_MB_DATA44	DB28	DDR1_DQ[44]		
MEM_MB_DATA43	DF34	DDR1_DQ[43]		
MEM_MB_DATA42	DC34	DDR1_DQ[42]		
MEM_MB_DATA41	DB30	DDR1_DQ[41]		
MEM_MB_DATA40	DA29	DDR1_DQ[40]		
MEM_MB_DATA39	CR31	DDR1_DQ[39]		
MEM_MB_DATA38	CU31	DDR1_DQ[38]		
MEM_MB_DATA37	CR27	DDR1_DQ[37]		
MEM_MB_DATA36	CU27	DDR1_DQ[36]		
MEM_MB_DATA35	CP32	DDR1_DQ[35]		
MEM_MB_DATA34	CT32	DDR1_DQ[34]		
MEM_MB_DATA33	CP28	DDR1_DQ[33]		
MEM_MB_DATA32	CT28	DDR1_DQ[32]		
MEM_MB_DATA31	DE10	DDR1_DQ[31]		
MEM_MB_DATA30	DE9	DDR1_DQ[30]		
MEM_MB_DATA29	CV6	DDR1_DQ[29]		
MEM_MB_DATA28	DA5	DDR1_DQ[28]		
MEM_MB_DATA27	DC11	DDR1_DQ[27]		
MEM_MB_DATA26	DE11	DDR1_DQ[26]		
MEM_MB_DATA25	DB8	DDR1_DQ[25]		
MEM_MB_DATA24	DA7	DDR1_DQ[24]		
MEM_MB_DATA23	CR5	DDR1_DQ[23]		
MEM_MB_DATA22	CU5	DDR1_DQ[22]		
MEM_MB_DATA21	CP2	DDR1_DQ[21]		
MEM_MB_DATA20	CR1	DDR1_DQ[20]		
MEM_MB_DATA19	CR6	DDR1_DQ[19]		
MEM_MB_DATA18	CT6	DDR1_DQ[18]		
MEM_MB_DATA17	CV2	DDR1_DQ[17]		
MEM_MB_DATA16	CR3	DDR1_DQ[16]		
MEM_MB_DATA15	CL3	DDR1_DQ[15]		
MEM_MB_DATA14	CK6	DDR1_DQ[14]		
MEM_MB_DATA13	CF8	DDR1_DQ[13]		
MEM_MB_DATA12	CE5	DDR1_DQ[12]		
MEM_MB_DATA11	CM4	DDR1_DQ[11]		
MEM_MB_DATA10	CL5	DDR1_DQ[10]		
MEM_MB_DATA9	CF4	DDR1_DQ[9]		
MEM_MB_DATA8	CE3	DDR1_DQ[8]		
MEM_MB_DATA7	BY2	DDR1_DQ[7]		
MEM_MB_DATA6	CA1	DDR1_DQ[6]		
MEM_MB_DATA5	B12	DDR1_DQ[5]		
MEM_MB_DATA4	B14	DDR1_DQ[4]		
MEM_MB_DATA3	CB4	DDR1_DQ[3]		
MEM_MB_DATA2	CA3	DDR1_DQ[2]		
MEM_MB_DATA1	BU1	DDR1_DQ[1]		
MEM_MB_DATA0	BV4	DDR1_DQ[0]		

DDR1_DQS_DP[17]	CW13
DDR1_DQS_DP[16]	DD36
DDR1_DQS_DP[15]	CV36
DDR1_DQS_DP[14]	DA31
DDR1_DQS_DP[13]	CU23
DDR1_DQS_DP[12]	DC7
DDR1_DQS_DP[11]	CW3
DDR1_DQS_DP[10]	CH4
DDR1_DQS_DP[9]	BV2
DDR1_DQS_DP[8]	DB14
DDR1_DQS_DP[7]	DB38
DDR1_DQS_DP[6]	CR37
DDR1_DQS_DP[5]	DD32
DDR1_DQS_DP[4]	CT30
DDR1_DQS_DP[3]	DB10
DDR1_DQS_DP[2]	CT4
DDR1_DQS_DP[1]	CJ5
DDR1_DQS_DP[0]	BY4
DDR1_DQS_DN[17]	CY14
DDR1_DQS_DN[16]	DE37
DDR1_DQS_DN[15]	CT35
DDR1_DQS_DN[14]	CY32
DDR1_DQS_DN[13]	CR23
DDR1_DQS_DN[12]	DD2
DDR1_DQS_DN[11]	CU3
DDR1_DQS_DN[10]	CG3
DDR1_DQS_DN[9]	BU11
DDR1_DQS_DN[8]	DA13
DDR1_DQS_DN[7]	DA37
DDR1_DQS_DN[6]	CU37
DDR1_DQS_DN[5]	DB32
DDR1_DQS_DN[4]	CV30
DDR1_DQS_DN[3]	DC9
DDR1_DQS_DN[2]	CH6
DDR1_DQS_DN[1]	CV4
DDR1_DQS_DN[0]	BW3
DDR1_MA[17]	CT24
DDR1_MA[16]	CY24
DDR1_MA[15]	CU24
DDR1_MA[14]	CU23
DDR1_MA[13]	CW25
DDR1_MA[12]	CW17
DDR1_MA[11]	CV18
DDR1_MA[10]	CR23
DDR1_MA[9]	CY18
DDR1_MA[8]	DA19
DDR1_MA[7]	CT18
DDR1_MA[6]	CW19
DDR1_MA[5]	CV20
DDR1_MA[4]	CR19
DDR1_MA[3]	CW21
DDR1_MA[2]	CV20
DDR1_MA[1]	DA21
DDR1_MA[0]	CY22
DDR1_CKE[5]	DA13
DDR1_CKE[4]	CV16
DDR1_CKE[3]	DE16
DDR1_CKE[2]	DD18
DDR1_CKE[1]	DC17
DDR1_CKE[0]	DA17
DDR1_ODT[5]	DD28
DDR1_ODT[4]	DA25
DDR1_ODT[3]	DC25
DDR1_ODT[2]	DC23
DDR1_ODT[1]	DE25
DDR1_ODT[0]	DD22
DDR1_CS_N[9]	DE28
DDR1_CS_N[8]	DE24
DDR1_CS_N[7]CID[4]	CV26
DDR1_CS_N[6]CID[3]	CV26
DDR1_CS_N[5]	CV26
DDR1_CS_N[4]	DD24
DDR1_CS_N[3]CID[1]	CP26
DDR1_CS_N[2]CID[0]	CT26
DDR1_CS_N[1]	DE23
DDR1_CS_N[0]	DE22
DDR1_CLK_DP[3]	CR25
DDR1_CLK_DP[2]	CT16
DDR1_CLK_DP[1]	CR15
DDR1_CLK_DP[0]	CT20
DDR1_CLK_DN[3]	
DDR1_CLK_DN[2]	
DDR1_CLK_DN[1]	
DDR1_CLK_DN[0]	
DDR1_BG[1]	
DDR1_BG[0]	
DDR1_BA[1]	
DDR1_BA[0]	

MEM\_MB\_ADD[17..0] ← MEM\_MB\_ADD[17..0] 16

16 MEM\_MB\_CLK2\_H ←

16 MEM\_MB\_CLK0\_H ←

16 MEM\_MB\_CLK2\_L ←

16 MEM\_MB\_CLK0\_L ←

16 MEM\_MB\_BG1 ←

16 MEM\_MB\_BG0 ←

16 MEM\_MB\_BA1 ←

16 MEM\_MB\_BA0 ←

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HSW-E MEMORY 2

Centauri

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17 MEM\_MC\_DATA[63..0] ← MEM\_MC\_DATA[63..0]

17 MEM\_MC\_CLK2\_H ←

17 MEM\_MC\_CLK0\_H ←

17 MEM\_MC\_CLK2\_L ←

17 MEM\_MC\_CLK0\_L ←

17 MEM\_MC\_BG1 ←

17 MEM\_MC\_BG0 ←

17 MEM\_MC\_BA1 ←

17 MEM\_MC\_BA0 ←

MEM\_MC\_DATA63 AL7  
MEM\_MC\_DATA62 AK8  
MEM\_MC\_DATA61 AE9  
MEM\_MC\_DATA60 AE7  
MEM\_MC\_DATA59 AL9  
MEM\_MC\_DATA58 AK10  
MEM\_MC\_DATA57 AG7  
MEM\_MC\_DATA56 AG8  
MEM\_MC\_DATA55 AL15  
MEM\_MC\_DATA54 AK14  
MEM\_MC\_DATA53 AF14  
MEM\_MC\_DATA52 AG15  
MEM\_MC\_DATA51 AL13  
MEM\_MC\_DATA50 AE12  
MEM\_MC\_DATA49 AE11  
MEM\_MC\_DATA48 Y8  
MEM\_MC\_DATA47 AA9  
MEM\_MC\_DATA46 U11  
MEM\_MC\_DATA45 T10  
MEM\_MC\_DATA44 AB8  
MEM\_MC\_DATA43 AA11  
MEM\_MC\_DATA42 W11  
MEM\_MC\_DATA41 U9  
MEM\_MC\_DATA40 M6  
MEM\_MC\_DATA39 K6  
MEM\_MC\_DATA38 L9  
MEM\_MC\_DATA37 J9  
MEM\_MC\_DATA36 P7  
MEM\_MC\_DATA35 R6  
MEM\_MC\_DATA34 K6  
MEM\_MC\_DATA33 N9  
MEM\_MC\_DATA32 T24  
MEM\_MC\_DATA31 V24  
MEM\_MC\_DATA30 T28  
MEM\_MC\_DATA29 V28  
MEM\_MC\_DATA28 R23  
MEM\_MC\_DATA27 U23  
MEM\_MC\_DATA26 R27  
MEM\_MC\_DATA25 U27  
MEM\_MC\_DATA24 AC31  
MEM\_MC\_DATA23 AE31  
MEM\_MC\_DATA22 AA35  
MEM\_MC\_DATA21 AC35  
MEM\_MC\_DATA20 AB30  
MEM\_MC\_DATA19 AB34  
MEM\_MC\_DATA18 AD34  
MEM\_MC\_DATA17 W31  
MEM\_MC\_DATA16 T32  
MEM\_MC\_DATA15 U35  
MEM\_MC\_DATA14 T30  
MEM\_MC\_DATA13 U33  
MEM\_MC\_DATA12 V30  
MEM\_MC\_DATA11 U33  
MEM\_MC\_DATA10 V34  
MEM\_MC\_DATA9 U37  
MEM\_MC\_DATA8 T38  
MEM\_MC\_DATA7 AC39  
MEM\_MC\_DATA6 AE37  
MEM\_MC\_DATA5 Y38  
MEM\_MC\_DATA4 R37  
MEM\_MC\_DATA3 AC37  
MEM\_MC\_DATA2 AD38  
MEM\_MC\_DATA1 AD38

CPU1D


HASWELL-E

DDR2\_DQ[63] AD26  
DDR2\_DQ[62] AH10  
DDR2\_DQ[61] V8  
DDR2\_DQ[60] M8  
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DDR2\_DQ[56] AB32  
DDR2\_DQ[55] AC25  
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DDR2\_DQ[53] AH12  
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DDR2\_DQ[46] AB26  
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DDR2\_DQ[18] U19  
DDR2\_DQ[17] M18  
DDR2\_DQ[16] P18  
DDR2\_DQ[15] R19  
DDR2\_DQ[14] L17  
DDR2\_DQ[13] T18  
DDR2\_DQ[12] M16  
DDR2\_DQ[11] L15  
DDR2\_DQ[10] AD22  
DDR2\_DQ[9] AB22  
DDR2\_DQ[8] Y22  
DDR2\_DQ[7] T22  
DDR2\_DQ[6] U21  
DDR2\_DQ[5] R21  
DDR2\_DQ[4] AD14  
DDR2\_DQ[3] AE17  
DDR2\_DQ[2] AB14  
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DDR2\_DQ[0] W15  
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MEM\_MC\_DQS\_H6 17  
MEM\_MC\_DQS\_H5 17  
MEM\_MC\_DQS\_H4 17  
MEM\_MC\_DQS\_H3 17  
MEM\_MC\_DQS\_H2 17  
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MEM\_MC\_ADD0  
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MEM\_MC\_CKE0 17  
MEM\_MC\_ODT1 17  
MEM\_MC\_ODT0 17  
MEM\_MC\_CS#3 17  
MEM\_MC\_CS#2 17  
MEM\_MC\_CS#1 17  
MEM\_MC\_CS#0 17  
MEM\_MC\_C2 17  
MEM\_MC\_ACT# 17  
MEM\_MC\_ALERT# 17  
MEM\_MC\_PAR 17

MEM\_MC\_ADD[17..0] ← MEM\_MC\_ADD[17..0] 17

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**MSI**  
Micro-Star International Co., Ltd.

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File

**HSW-E MEMORY 3**

Size

Document Number

Rev

**Centauri**

**A00**

Date: Friday, June 06, 2014

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				CPU/F			
				HASWELL-E			
20	DMI_TX3	C307	C0.1u1604002	DMI_TX3	D42	DMI_TX_DP[3]	E47
20	DMI_TX2	C305	C0.1u1604002	DMI_TX2	E43	DMI_TX_DP[2]	D48
20	DMI_TX1	C333	C0.1u1604002	DMI_TX1	D44	DMI_TX_DP[1]	E49
20	DMI_TX0	C331	C0.1u1604002	DMI_TX0	E45	DMI_TX_DP[0]	D50
20	DMI_TX0M	C336	C0.1u1604002	DMI_TX0M	B42	DMI_TX_DN[3]	C47
20	DMI_TX0P	C336	C0.1u1604002	DMI_TX0P	C43	DMI_TX_DN[2]	B48
20	DMI_TX0I	C334	C0.1u1604002	DMI_TX0I	B44	DMI_TX_DN[1]	C49
20	DMI_TX0M	C332	C0.1u1604002	DMI_TX0M	C45	DMI_TX_DN[0]	B50
30	EXP_C_TXP_7	L48		PE1B_RX_DP[7]		EXP_C_RXP_7	M56
30	EXP_C_TXP_6	K46		PE1B_RX_DP[6]		EXP_C_RXP_6	L57
30	EXP_C_TXP_5	L47		PE1B_RX_DP[5]		EXP_C_RXP_5	M54
30	EXP_C_TXP_4	K46		PE1B_RX_DP[4]		EXP_C_RXP_4	L53
30	EXP_C_TXN_7	J49		PE1B_RX_DN[7]		EXP_C_RXN_7	K56
30	EXP_C_TXN_6	H46		PE1B_RX_DN[6]		EXP_C_RXN_6	J57
30	EXP_C_TXN_5	J47		PE1B_RX_DN[5]		EXP_C_RXN_5	K54
30	EXP_C_TXN_4	H46		PE1B_RX_DN[4]		EXP_C_RXN_4	J53
30	EXP_C_TXP_3	L45		PE1A_RX_DP[3]		EXP_C_RXP_3	G55
30	EXP_C_TXP_2	K44		PE1A_RX_DP[2]		EXP_C_RXP_2	F54
30	EXP_C_TXP_1	L43		PE1A_RX_DP[1]		EXP_C_RXP_1	E52
30	EXP_C_TXP_0	K42		PE1A_RX_DP[0]		EXP_C_RXP_0	F51
30	EXP_C_TXN_3	J45		PE1A_RX_DN[3]		EXP_C_RXN_3	E55
30	EXP_C_TXN_2	H44		PE1A_RX_DN[2]		EXP_C_RXN_2	D54
30	EXP_C_TXN_1	J43		PE1A_RX_DN[1]		EXP_C_RXN_1	D52
30	EXP_C_TXN_0	H42		PE1A_RX_DN[0]		EXP_C_RXN_0	C51
26	EXP_A_TXP_15	BA47		PE2D_TX_DP[15]		EXP_A_RXP_15	B656
26	EXP_A_TXP_14	AY48		PE2D_TX_DP[14]		EXP_A_RXP_14	BA57
26	EXP_A_TXP_13	BA49		PE2D_TX_DP[13]		EXP_A_RXP_13	AT56
26	EXP_A_TXP_12	AY50		PE2D_TX_DP[12]		EXP_A_RXP_12	AY58
26	EXP_A_TXN_15	AW47		PE2D_TX_DN[15]		EXP_A_RXN_15	AY56
26	EXP_A_TXN_14	AV48		PE2D_TX_DN[14]		EXP_A_RXN_14	AY58
26	EXP_A_TXN_13	AW49		PE2D_TX_DN[13]		EXP_A_RXN_13	AY56
26	EXP_A_TXN_12	AV50		PE2D_TX_DN[12]		EXP_A_RXN_12	AT58
26	EXP_A_TXP_11	BA51		PE2C_TX_DP[11]		EXP_A_RXP_11	AL57
26	EXP_A_TXP_10	B854		PE2C_TX_DP[10]		EXP_A_RXP_10	AL57
26	EXP_A_TXP_9	BA53		PE2C_TX_DP[9]		EXP_A_RXP_9	AK56
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26	EXP_A_TXN_8	AY52		PE2C_TX_DN[8]		EXP_A_RXN_8	AK56
26	EXP_A_TXP_7	AT54		PE2B_TX_DP[7]		EXP_A_RXP_7	AF58
26	EXP_A_TXP_6	AR53		PE2B_TX_DP[6]		EXP_A_RXP_6	AE58
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26	EXP_A_TXP_4	AE53		PE2B_TX_DP[4]		EXP_A_RXP_4	AE54
26	EXP_A_TXN_7	AP54		PE2B_TX_DN[7]		EXP_A_RXN_7	AE57
26	EXP_A_TXN_6	AN53		PE2B_TX_DN[6]		EXP_A_RXN_6	AC56
26	EXP_A_TXN_5	AP54		PE2B_TX_DN[5]		EXP_A_RXN_5	AE54
26	EXP_A_TXN_4	AE53		PE2B_TX_DN[4]		EXP_A_RXN_4	AE54
26	EXP_A_TXP_3	AP52		PE2A_TX_DP[3]		EXP_A_RXP_3	W55
26	EXP_A_TXP_2	AR51		PE2A_TX_DP[2]		EXP_A_RXP_2	V56
26	EXP_A_TXP_1	AP50		PE2A_TX_DP[1]		EXP_A_RXP_1	V54
26	EXP_A_TXP_0	AR49		PE2A_TX_DP[0]		EXP_A_RXP_0	N55
26	EXP_A_TXN_3	AM52		PE2A_TX_DN[3]		EXP_A_RXN_3	W55
26	EXP_A_TXN_2	AN51		PE2A_TX_DN[2]		EXP_A_RXN_2	T54
26	EXP_A_TXN_1	AM50		PE2A_TX_DN[1]		EXP_A_RXN_1	T54
26	EXP_A_TXN_0	AM49		PE2A_TX_DN[0]		EXP_A_RXN_0	W55

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				CPU/G			
				HASWELL-E			
26	EXP_B_TXP_15	P44		PE3D_TX_DP[15]		EXP_B_RXP_15	AR46
26	EXP_B_TXP_14	AA43		PE3D_TX_DP[14]		EXP_B_RXP_14	AR46
26	EXP_B_TXP_13	AA44		PE3D_TX_DP[13]		EXP_B_RXP_13	AR47
26	EXP_B_TXP_12	AC45		PE3D_TX_DP[12]		EXP_B_RXP_12	AR47
26	EXP_B_TXN_15	T44		PE3D_TX_DN[15]		EXP_B_RXN_15	AM45
26	EXP_B_TXN_14	AC43		PE3D_TX_DN[14]		EXP_B_RXN_14	AM46
26	EXP_B_TXN_13	Y44		PE3D_TX_DN[13]		EXP_B_RXN_13	AM47
26	EXP_B_TXN_12	AA45		PE3D_TX_DN[12]		EXP_B_RXN_12	AG47
26	EXP_B_TXP_11	AB46		PE3C_TX_DP[11]		EXP_B_RXP_11	AJ49
26	EXP_B_TXP_10	AC47		PE3C_TX_DP[10]		EXP_B_RXP_10	AE50
26	EXP_B_TXP_9	U45		PE3C_TX_DP[9]		EXP_B_RXP_9	AE51
26	EXP_B_TXP_8	T46		PE3C_TX_DP[8]		EXP_B_RXP_8	AH48
26	EXP_B_TXN_11	Y46		PE3C_TX_DN[11]		EXP_B_RXN_11	AG49
26	EXP_B_TXN_10	AA47		PE3C_TX_DN[10]		EXP_B_RXN_10	AE50
26	EXP_B_TXN_9	R46		PE3C_TX_DN[9]		EXP_B_RXN_9	AG51
26	EXP_B_TXN_8	P46		PE3C_TX_DN[8]		EXP_B_RXN_8	AE48
26	EXP_B_TXP_7	U49		PE3B_TX_DP[7]		EXP_B_RXP_7	AC51
26	EXP_B_TXP_6	T50		PE3B_TX_DP[6]		EXP_B_RXP_6	AC53
26	EXP_B_TXP_5	U51		PE3B_TX_DP[5]		EXP_B_RXP_5	AB52
26	EXP_B_TXP_4	T52		PE3B_TX_DP[4]		EXP_B_RXP_4	AB50
26	EXP_B_TXN_7	R49		PE3B_TX_DN[7]		EXP_B_RXN_7	AA51
26	EXP_B_TXN_6	P50		PE3B_TX_DN[6]		EXP_B_RXN_6	AA53
26	EXP_B_TXN_5	R51		PE3B_TX_DN[5]		EXP_B_RXN_5	Y52
26	EXP_B_TXN_4	T46		PE3B_TX_DN[4]		EXP_B_RXN_4	Y50
26	EXP_B_TXP_3	U47		PE3A_TX_DP[3]		EXP_B_RXP_3	AC49
26	EXP_B_TXP_2	L51		PE3A_TX_DP[2]		EXP_B_RXP_2	AH46
26	EXP_B_TXP_1	K50		PE3A_TX_DP[1]		EXP_B_RXP_1	AJ45
26	EXP_B_TXP_0	K50		PE3A_TX_DP[0]		EXP_B_RXP_0	AH44
26	EXP_B_TXN_3	P48		PE3A_TX_DN[3]		EXP_B_RXN_3	AA49
26	EXP_B_TXN_2	R47		PE3A_TX_DN[2]		EXP_B_RXN_2	AE46
26	EXP_B_TXN_1	J51		PE3A_TX_DN[1]		EXP_B_RXN_1	AG45
26	EXP_B_TXN_0	H50		PE3A_TX_DN[0]		EXP_B_RXN_0	AE44

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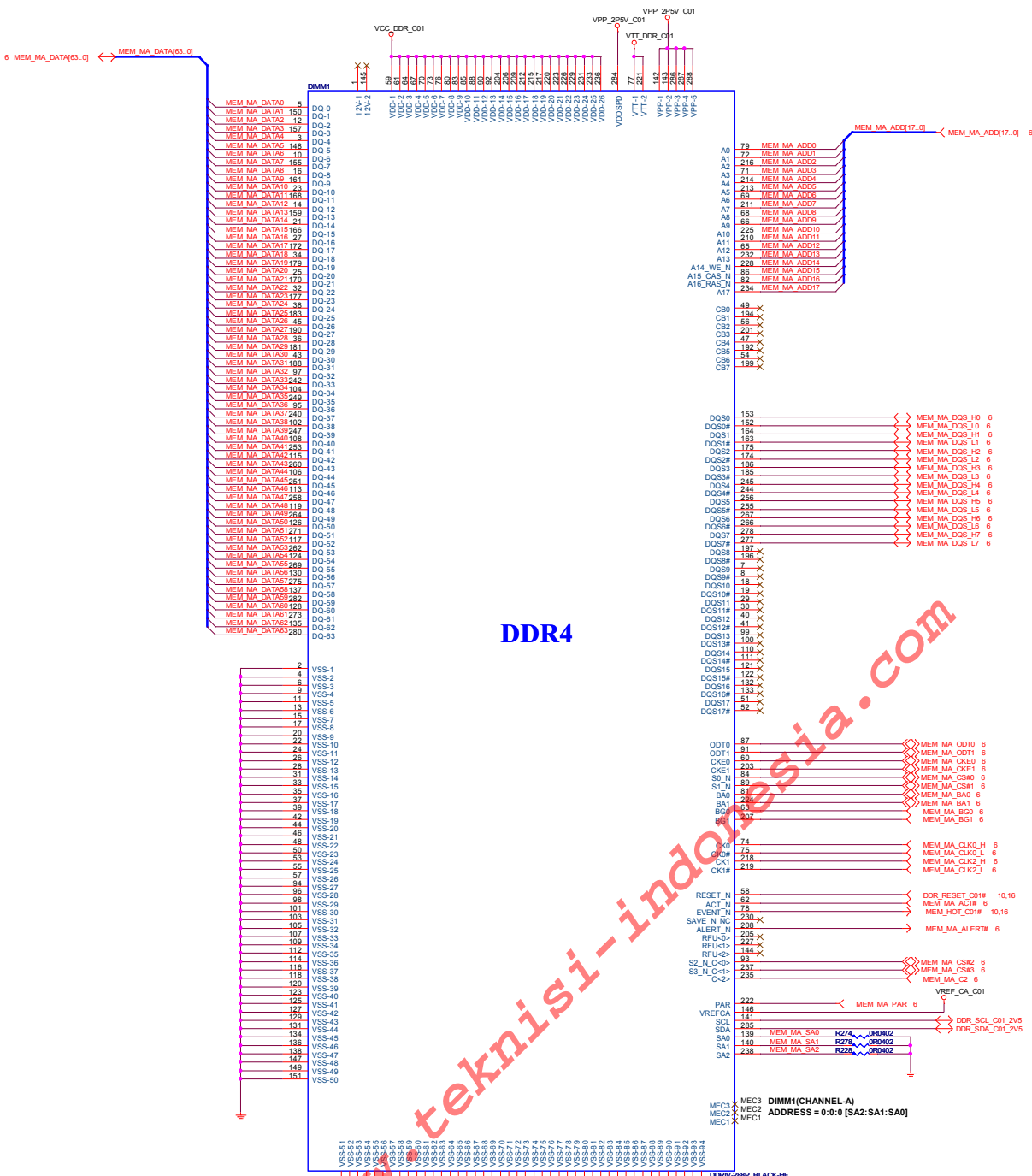
 <b>MICRO-START INT'L CO.,LTD.</b>		
Title <b>HSW-E PCIE/DMI</b>		
Size	Document Number	Rev <b>A00</b>
<b>Centauri</b>		
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HASWELL-E

CH12	VSS-167	CUI1	VSS-78	BC47	VSS-315	BW15	Y36	VSS-472	VSS-394	A23	VSS-629	M2	VSS-553
CH35	VSS-158	CUI2	VSS-77	BC48	VSS-314	BW17	Y4	VSS-480	VSS-393	A24	VSS-628	M3	VSS-552
CH58	VSS-155	CUI3	VSS-76	BC49	VSS-313	BW43	Y5	VSS-471	VSS-392	A25	VSS-627	M4	VSS-551
CH82	VSS-153	CUI4	VSS-75	BC51	VSS-312	BW44	Y6	VSS-470	VSS-391	A26	VSS-626	M5	VSS-550
CH105	VSS-150	CUI5	VSS-74	BC52	VSS-311	BW45	Y7	VSS-469	VSS-390	A27	VSS-625	M6	VSS-549
CH128	VSS-147	CUI6	VSS-73	BC53	VSS-310	BW46	Y8	VSS-468	VSS-389	A28	VSS-624	M7	VSS-548
CH151	VSS-145	CUI7	VSS-72	BC54	VSS-309	BW47	Y9	VSS-467	VSS-388	A29	VSS-623	M8	VSS-547
CH174	VSS-144	CUI8	VSS-71	BC55	VSS-308	BW48	Y10	VSS-466	VSS-387	A30	VSS-622	M9	VSS-546
CH197	VSS-143	CUI9	VSS-70	BC56	VSS-307	BW49	Y11	VSS-465	VSS-386	A31	VSS-621	M10	VSS-545
CH220	VSS-142	CUI10	VSS-69	BC57	VSS-306	BW50	Y12	VSS-464	VSS-385	A32	VSS-620	M11	VSS-544
CH243	VSS-141	CUI11	VSS-68	BC58	VSS-305	BW51	Y13	VSS-463	VSS-384	A33	VSS-619	M12	VSS-543
CH266	VSS-140	CUI12	VSS-67	BC59	VSS-304	BW52	Y14	VSS-462	VSS-383	A34	VSS-618	M13	VSS-542
CH289	VSS-139	CUI13	VSS-66	BC60	VSS-303	BW53	Y15	VSS-461	VSS-382	A35	VSS-617	M14	VSS-541
CH312	VSS-138	CUI14	VSS-65	BC61	VSS-302	BW54	Y16	VSS-460	VSS-381	A36	VSS-616	M15	VSS-540
CH335	VSS-137	CUI15	VSS-64	BC62	VSS-301	BW55	Y17	VSS-459	VSS-380	A37	VSS-615	M16	VSS-539
CH358	VSS-136	CUI16	VSS-63	BC63	VSS-300	BW56	Y18	VSS-458	VSS-379	A38	VSS-614	M17	VSS-538
CH381	VSS-135	CUI17	VSS-62	BC64	VSS-299	BW57	Y19	VSS-457	VSS-378	A39	VSS-613	M18	VSS-537
CH404	VSS-134	CUI18	VSS-61	BC65	VSS-298	BW58	Y20	VSS-456	VSS-377	A40	VSS-612	M19	VSS-536
CH427	VSS-133	CUI19	VSS-60	BC66	VSS-297	BW59	Y21	VSS-455	VSS-376	A41	VSS-611	M20	VSS-535
CH450	VSS-132	CUI20	VSS-59	BC67	VSS-296	BW60	Y22	VSS-454	VSS-375	A42	VSS-610	M21	VSS-534
CH473	VSS-131	CUI21	VSS-58	BC68	VSS-295	BW61	Y23	VSS-453	VSS-374	A43	VSS-609	M22	VSS-533
CH496	VSS-130	CUI22	VSS-57	BC69	VSS-294	BW62	Y24	VSS-452	VSS-373	A44	VSS-608	M23	VSS-532
CH519	VSS-129	CUI23	VSS-56	BC70	VSS-293	BW63	Y25	VSS-451	VSS-372	A45	VSS-607	M24	VSS-531
CH542	VSS-128	CUI24	VSS-55	BC71	VSS-292	BW64	Y26	VSS-450	VSS-371	A46	VSS-606	M25	VSS-530
CH565	VSS-127	CUI25	VSS-54	BC72	VSS-291	BW65	Y27	VSS-449	VSS-370	A47	VSS-605	M26	VSS-529
CH588	VSS-126	CUI26	VSS-53	BC73	VSS-290	BW66	Y28	VSS-448	VSS-369	A48	VSS-604	M27	VSS-528
CH611	VSS-125	CUI27	VSS-52	BC74	VSS-289	BW67	Y29	VSS-447	VSS-368	A49	VSS-603	M28	VSS-527
CH634	VSS-124	CUI28	VSS-51	BC75	VSS-288	BW68	Y30	VSS-446	VSS-367	A50	VSS-602	M29	VSS-526
CH657	VSS-123	CUI29	VSS-50	BC76	VSS-287	BW69	Y31	VSS-445	VSS-366	A51	VSS-601	M30	VSS-525
CH680	VSS-122	CUI30	VSS-49	BC77	VSS-286	BW70	Y32	VSS-444	VSS-365	A52	VSS-600	M31	VSS-524
CH703	VSS-121	CUI31	VSS-48	BC78	VSS-285	BW71	Y33	VSS-443	VSS-364	A53	VSS-599	M32	VSS-523
CH726	VSS-120	CUI32	VSS-47	BC79	VSS-284	BW72	Y34	VSS-442	VSS-363	A54	VSS-598	M33	VSS-522
CH749	VSS-119	CUI33	VSS-46	BC80	VSS-283	BW73	Y35	VSS-441	VSS-362	A55	VSS-597	M34	VSS-521
CH772	VSS-118	CUI34	VSS-45	BC81	VSS-282	BW74	Y36	VSS-440	VSS-361	A56	VSS-596	M35	VSS-520
CH795	VSS-117	CUI35	VSS-44	BC82	VSS-281	BW75	Y37	VSS-439	VSS-360	A57	VSS-595	M36	VSS-519
CH818	VSS-116	CUI36	VSS-43	BC83	VSS-280	BW76	Y38	VSS-438	VSS-359	A58	VSS-594	M37	VSS-518
CH841	VSS-115	CUI37	VSS-42	BC84	VSS-279	BW77	Y39	VSS-437	VSS-358	A59	VSS-593	M38	VSS-517
CH864	VSS-114	CUI38	VSS-41	BC85	VSS-278	BW78	Y40	VSS-436	VSS-357	A60	VSS-592	M39	VSS-516
CH887	VSS-113	CUI39	VSS-40	BC86	VSS-277	BW79	Y41	VSS-435	VSS-356	A61	VSS-591	M40	VSS-515
CH910	VSS-112	CUI40	VSS-39	BC87	VSS-276	BW80	Y42	VSS-434	VSS-355	A62	VSS-590	M41	VSS-514
CH933	VSS-111	CUI41	VSS-38	BC88	VSS-275	BW81	Y43	VSS-433	VSS-354	A63	VSS-589	M42	VSS-513
CH956	VSS-110	CUI42	VSS-37	BC89	VSS-274	BW82	Y44	VSS-432	VSS-353	A64	VSS-588	M43	VSS-512
CH979	VSS-109	CUI43	VSS-36	BC90	VSS-273	BW83	Y45	VSS-431	VSS-352	A65	VSS-587	M44	VSS-511
CH1002	VSS-108	CUI44	VSS-35	BC91	VSS-272	BW84	Y46	VSS-430	VSS-351	A66	VSS-586	M45	VSS-510
CH1025	VSS-107	CUI45	VSS-34	BC92	VSS-271	BW85	Y47	VSS-429	VSS-350	A67	VSS-585	M46	VSS-509
CH1048	VSS-106	CUI46	VSS-33	BC93	VSS-270	BW86	Y48	VSS-428	VSS-349	A68	VSS-584	M47	VSS-508
CH1071	VSS-105	CUI47	VSS-32	BC94	VSS-269	BW87	Y49	VSS-427	VSS-348	A69	VSS-583	M48	VSS-507
CH1094	VSS-104	CUI48	VSS-31	BC95	VSS-268	BW88	Y50	VSS-426	VSS-347	A70	VSS-582	M49	VSS-506
CH1117	VSS-103	CUI49	VSS-30	BC96	VSS-267	BW89	Y51	VSS-425	VSS-346	A71	VSS-581	M50	VSS-505
CH1140	VSS-102	CUI50	VSS-29	BC97	VSS-266	BW90	Y52	VSS-424	VSS-345	A72	VSS-580	M51	VSS-504
CH1163	VSS-101	CUI51	VSS-28	BC98	VSS-265	BW91	Y53	VSS-423	VSS-344	A73	VSS-579	M52	VSS-503
CH1186	VSS-100	CUI52	VSS-27	BC99	VSS-264	BW92	Y54	VSS-422	VSS-343	A74	VSS-578	M53	VSS-502
CH1209	VSS-99	CUI53	VSS-26	BC100	VSS-263	BW93	Y55	VSS-421	VSS-342	A75	VSS-577	M54	VSS-501
CH1232	VSS-98	CUI54	VSS-25	BC101	VSS-262	BW94	Y56	VSS-420	VSS-341	A76	VSS-576	M55	VSS-500
CH1255	VSS-97	CUI55	VSS-24	BC102	VSS-261	BW95	Y57	VSS-419	VSS-340	A77	VSS-575	M56	VSS-499
CH1278	VSS-96	CUI56	VSS-23	BC103	VSS-260	BW96	Y58	VSS-418	VSS-339	A78	VSS-574	M57	VSS-498
CH1301	VSS-95	CUI57	VSS-22	BC104	VSS-259	BW97	Y59	VSS-417	VSS-338	A79	VSS-573	M58	VSS-497
CH1324	VSS-94	CUI58	VSS-21	BC105	VSS-258	BW98	Y60	VSS-416	VSS-337	A80	VSS-572	M59	VSS-496
CH1347	VSS-93	CUI59	VSS-20	BC106	VSS-257	BW99	Y61	VSS-415	VSS-336	A81	VSS-571	M60	VSS-495
CH1370	VSS-92	CUI60	VSS-19	BC107	VSS-256	BW100	Y62	VSS-414	VSS-335	A82	VSS-570	M61	VSS-494
CH1393	VSS-91	CUI61	VSS-18	BC108	VSS-255	BW101	Y63	VSS-413	VSS-334	A83	VSS-569	M62	VSS-493
CH1416	VSS-90	CUI62	VSS-17	BC109	VSS-254	BW102	Y64	VSS-412	VSS-333	A84	VSS-568	M63	VSS-492
CH1439	VSS-89	CUI63	VSS-16	BC110	VSS-253	BW103	Y65	VSS-411	VSS-332	A85	VSS-567	M64	VSS-491
CH1462	VSS-88	CUI64	VSS-15	BC111	VSS-252	BW104	Y66	VSS-410	VSS-331	A86	VSS-566	M65	VSS-490
CH1485	VSS-87	CUI65	VSS-14	BC112	VSS-251	BW105	Y67	VSS-409	VSS-330	A87	VSS-565	M66	VSS-489
CH1508	VSS-86	CUI66	VSS-13	BC113	VSS-250	BW106	Y68	VSS-408	VSS-329	A88	VSS-564	M67	VSS-488
CH1531	VSS-85	CUI67	VSS-12	BC114	VSS-249	BW107	Y69	VSS-407	VSS-328	A89	VSS-563	M68	VSS-487
CH1554	VSS-84	CUI68	VSS-11	BC115	VSS-248	BW108	Y70	VSS-406	VSS-327	A90	VSS-562	M69	VSS-486
CH1577	VSS-83	CUI69	VSS-10	BC116	VSS-247	BW109	Y71	VSS-405	VSS-326	A91	VSS-561	M70	VSS-485
CH1600	VSS-82	CUI70	VSS-9	BC117	VSS-246	BW110	Y72	VSS-404	VSS-325	A92	VSS-560	M71	VSS-484
CH1623	VSS-81	CUI71	VSS-8	BC118	VSS-245	BW111	Y73	VSS-403	VSS-324	A93	VSS-559	M72	VSS-483
CH1646	VSS-80	CUI72	VSS-7	BC119	VSS-244	BW112	Y74	VSS-402	VSS-323	A94	VSS-558	M73	VSS-482
CH1669	VSS-79	CUI73	VSS-6	BC120	VSS-243	BW113	Y75	VSS-401	VSS-322	A95	VSS-557	M74	VSS-481
CH1692	VSS-78	CUI74	VSS-5	BC121	VSS-242	BW114	Y76	VSS-400	VSS-321	A96	VSS-556	M75	VSS-480
CH1715	VSS-77	CUI75	VSS-4	BC122	VSS-241	BW115	Y77	VSS-399	VSS-320	A97	VSS-555	M76	VSS-479
CH1738	VSS-76	CUI76	VSS-3	BC123	VSS-240	BW116	Y78	VSS-398	VSS-319	A98	VSS-554	M77	VSS-478
CH1761	VSS-75	CUI77	VSS-2	BC124	VSS-239	BW117	Y79	VSS-397	VSS-318	A99	VSS-553	M78	VSS-477
CH1784	VSS-74	CUI78	VSS-1	BC125	VSS-238	BW118	Y80	VSS-396	VSS-317	A100	VSS-552	M79	VSS-476
CH1807	VSS-73	CUI79	VSS-0	BC126	VSS-237	BW119	Y81	VSS-395	VSS-316	A101	VSS-551	M80	VSS-475
CH1830	VSS-72	CUI80	VSS-0	BC127	VSS-236	BW120	Y82	VSS-394	VSS-315	A102	VSS-550	M81	VSS-474
CH1853	VSS-71	CUI81	VSS-0	BC128	VSS-235	BW121	Y83	VSS-393	VSS-314	A103	VSS-549	M82	VSS-473
CH1876	VSS-70	CUI82	VSS-0	BC129	VSS-234	BW122	Y84	VSS-392	VSS-313	A104	VSS-548	M83	VSS-472
CH1899	VSS-69	CUI83	VSS-0	BC130	VSS-233	BW123	Y85	VSS-391	VSS-312	A105	VSS-547	M84	VSS-471
CH1922	VSS-68	CUI84	VSS-0	BC131	VSS-232	BW124	Y86	VSS-390	VSS-311	A106	VSS-546	M85	VSS-470
CH1945	VSS-67	CUI85	VSS-0	BC132	VSS-231	BW125	Y87	VSS-389	VSS-310	A107	VSS-545	M86	VSS-469
CH1968	VSS-66	CUI86	VSS-0	BC133	VSS-230	BW126	Y88	VSS-388	VSS-309	A108	VSS-544	M87	VSS-468
CH1991	VSS-65	CUI87	VSS-0	BC134	VSS-229	BW127	Y89	VSS-387	VSS-308	A109	VSS-543	M88	VSS-467
CH2014	VSS-64	CUI88	VSS-0	BC135	VSS-228	BW128	Y90	VSS-386	VSS-307	A110	VSS-542	M89	VSS-466
CH2037	VSS-63	CUI89	VSS-0	BC136	VSS-227	BW129	Y91	VSS-385	VSS-306	A111	VSS-541	M90	VSS-465
CH2060	VSS-62	CUI90	VSS-0	BC137	VSS-226	BW130	Y92	VSS-384	VSS-305	A112	VSS-540	M91	VSS-464
CH2083	VSS-61	CUI91	VSS-0	BC138	VSS-225	BW131	Y93	VSS-383	VSS-304	A113	VSS-539	M92	VSS-463
CH2106	VSS-60	CUI92	VSS-0	BC139	VSS-224	BW132	Y94	VSS-382	VSS-303	A114	VSS-538	M93	VSS-462
CH2129	VSS-59	CUI93	VSS-0	BC140	VSS-223	BW133	Y95	VSS-381	VSS-302	A115	VSS-537	M94	VSS-461
CH2152	VSS-58	CUI94	VSS-0	BC141	VSS-222	BW134	Y96	VSS-380	VSS-301	A116	VSS-536	M95	VSS-460
CH2175	VSS-57	CUI95	VSS-0	BC142	VSS-221	BW135	Y97	VSS-379	VSS-300	A117	VSS-535	M96	VSS-459
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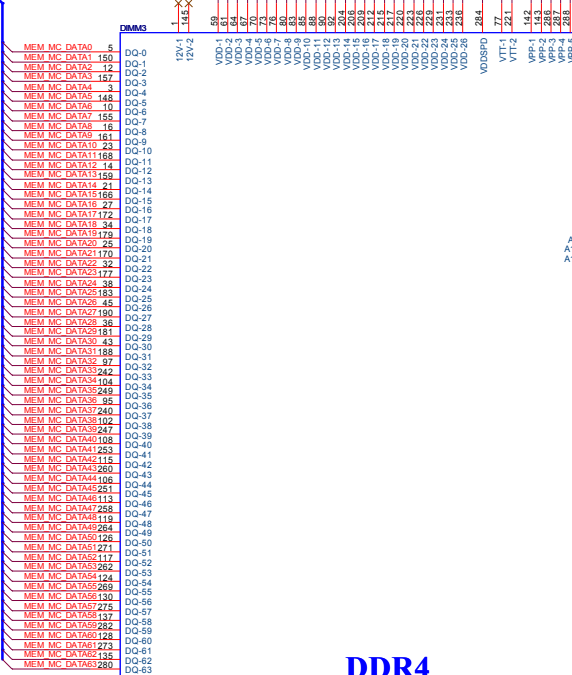






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VCC\_DDR\_C23  
VPP\_2P5V\_C23  
VTT\_DDR\_C23



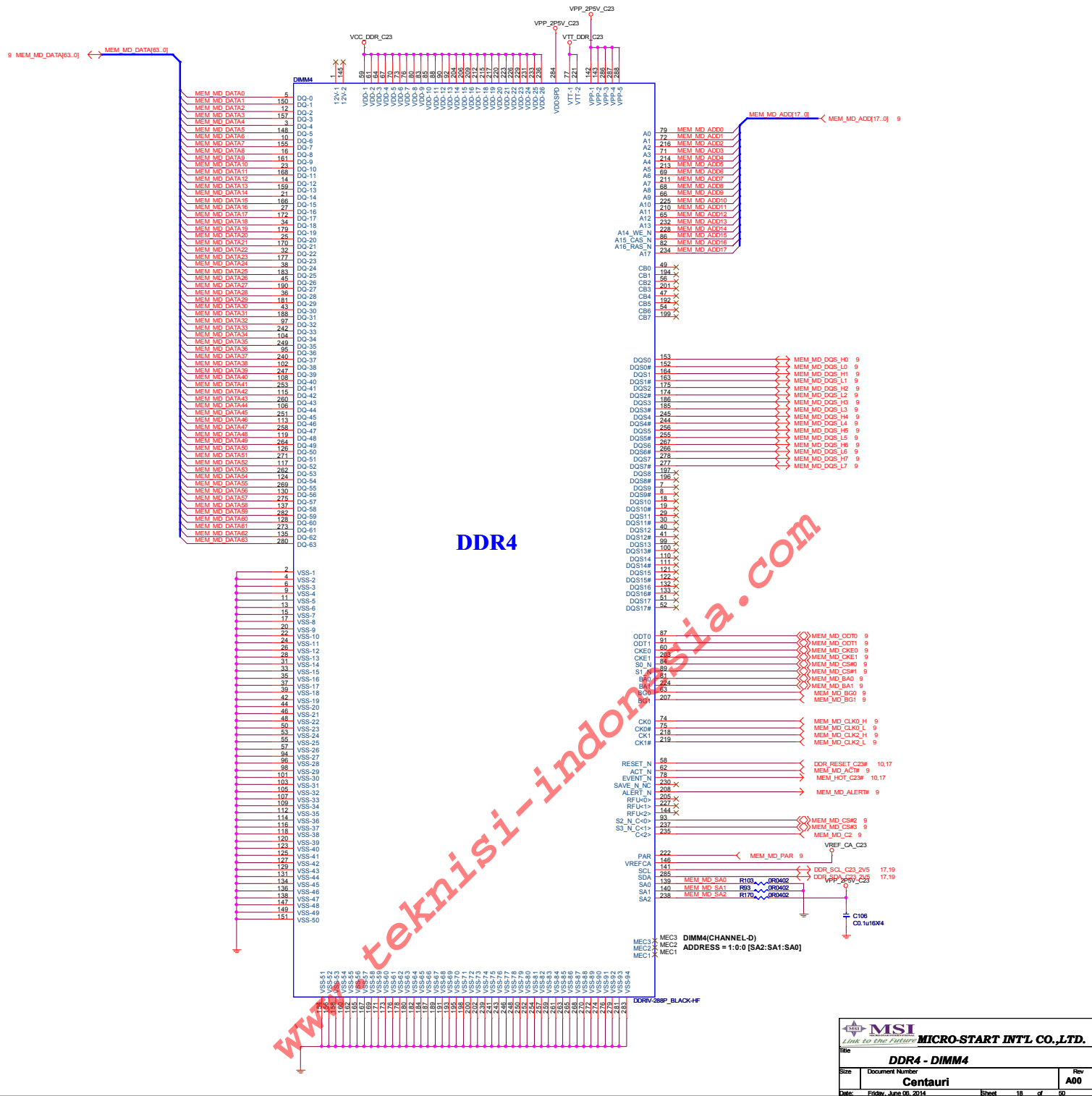
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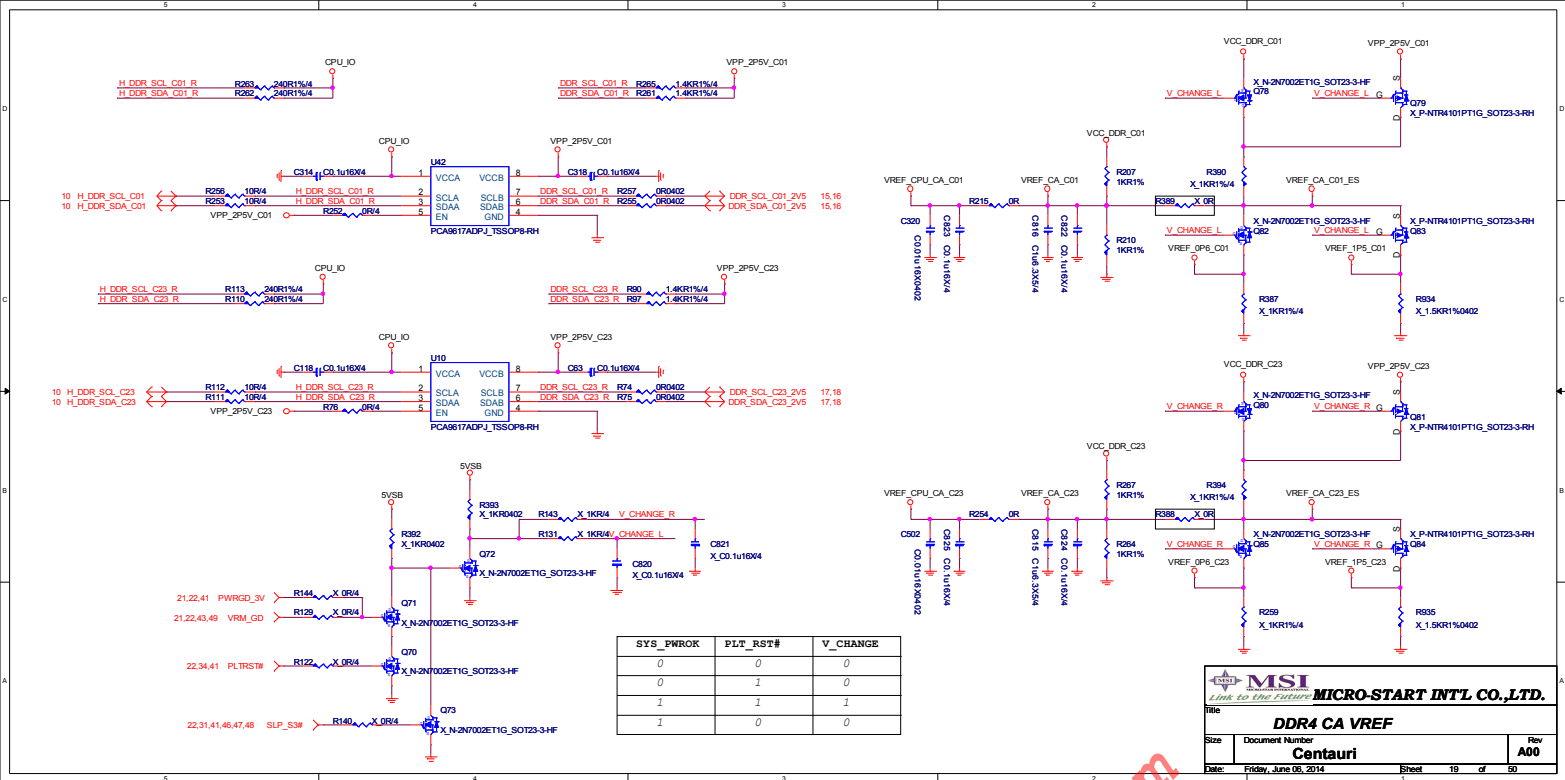


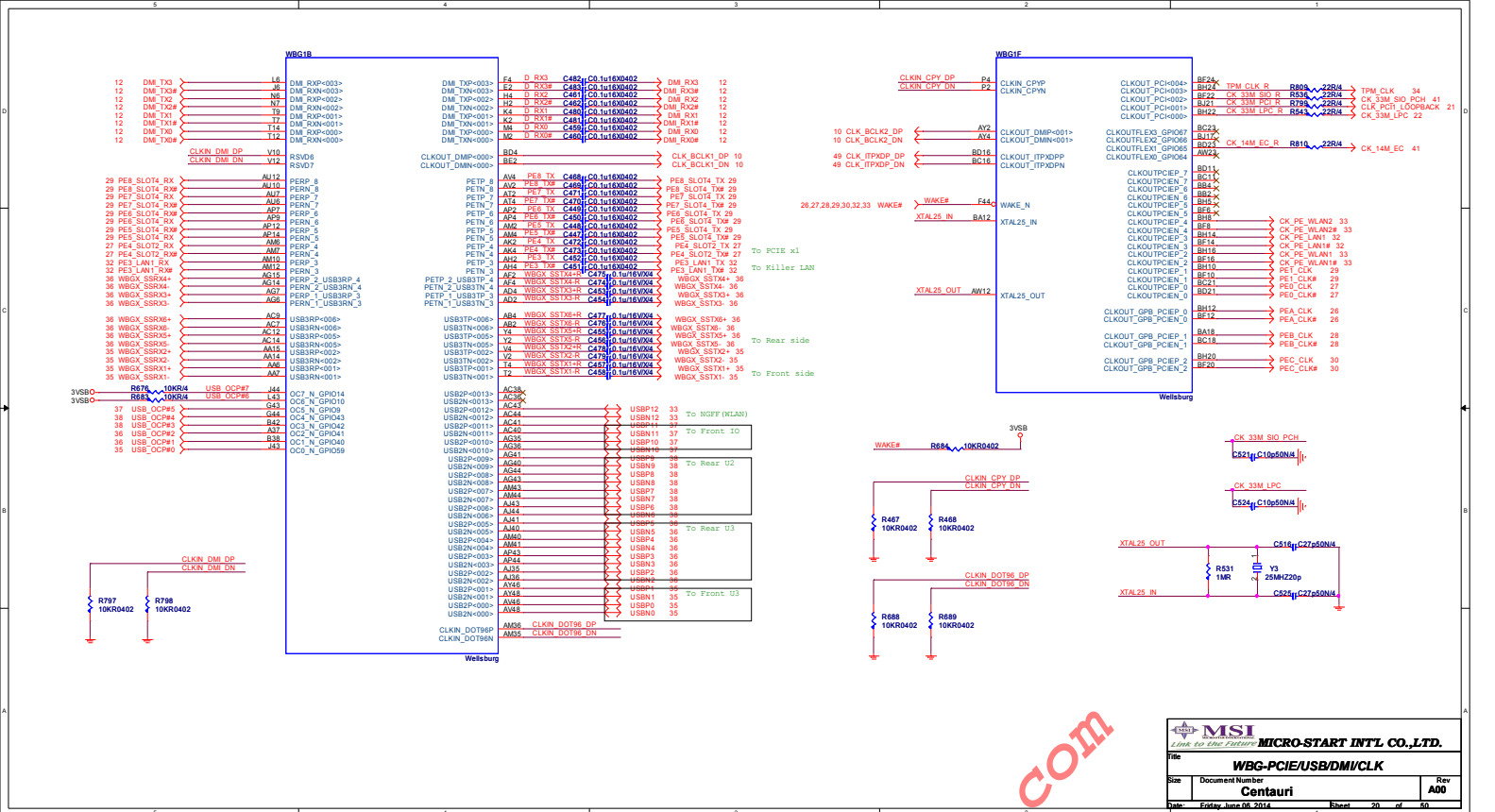
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DDR4 - DIMM3  
ADDRESS = 0:0:0 [SA2:SA1:SA0]

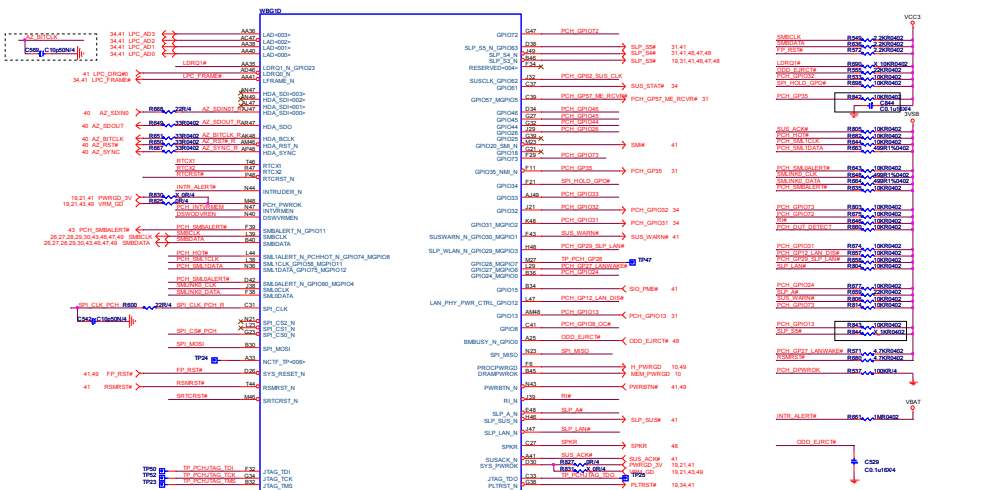
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Title <b>DDR4 - DIMM3</b>		
Size	Document Number	Rev <b>A00</b>
Date Friday, June 06, 2014		Sheet 17 of 50





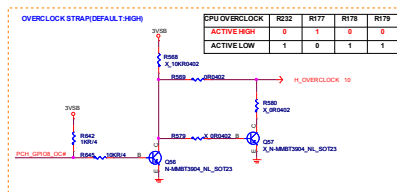






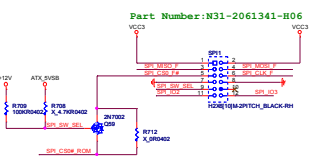
# REQUIRED STRAPS

PCH_GPIO0	R808	10K0402	QVAT	PLL ON DIE VIBR ENABLE HIGH PLL ON DIE VIBR ENABLE (DEFAULT) LOW PLL ON DIE VIBR DISABLE
PCH_GPIO1	R809	10K0402	QVAT	INTEGRATED SUB 1.8V VIBR ENABLE HIGH ENABLE (INTERNAL SUPPLY) (DEFAULT) LOW DISABLE (EXTERNAL SUPPLY)
PCH_GPIO2	R810	10K0402	QVAT	DEEP SLEEP WELL ON DIE VIBR ENABLE HIGH ENABLE (INTERNAL SUPPLY) (DEFAULT) LOW DISABLE (EXTERNAL SUPPLY)
PCH_GPIO3	R811	10K0402	QVAT	JTAG CLK FILTER BYPASS (SPA) HIGH NORMAL MODE (DEFAULT) LOW JTAG CLK FILTER BYPASS
PCH_GPIO4	R812	10K0402	QVAT	JTAG CLK FILTER BYPASS (SPA) HIGH NORMAL MODE (DEFAULT) LOW JTAG CLK FILTER BYPASS
PCH_GPIO5	R813	10K0402	QVAT	NO OSCILLATOR BYPASS (SPA) HIGH NORMAL MODE (DEFAULT) LOW RING OSCILLATOR BYPASS
PCH_GPIO6	R814	10K0402	QVAT	JTAG TRIGGER/READER
PCH_GPIO7	R815	10K0402	QVAT	When operating in DC-coupled mode: S = BM178 is term related to VSS S = BM178 is term related to VSS
PCH_GPIO8	R816	10K0402	QVAT	INTEGRATED CLOCK ENABLE HIGH DISABLE LOW ENABLE
PCH_GPIO9	R817	10K0402	QVAT	NO REBOOT OPTION STRAP HIGH NO REBOOT LOW REBOOT



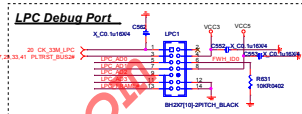
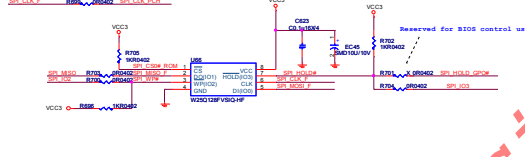
## SPI DEBUG PROT

Close to SPI ROM



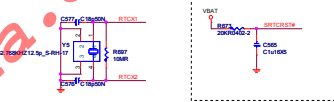
## SPI FLASH ROM

Place close to SB.



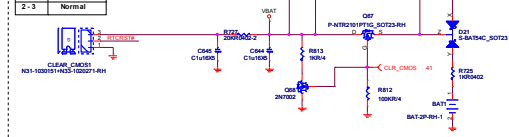
## RTC Block

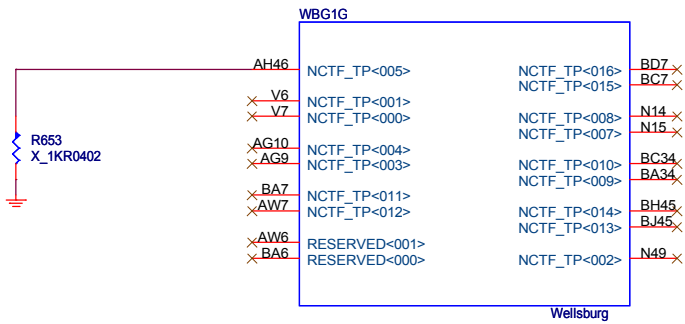
Close to PCH




## CLEAR CMOS JUMPER

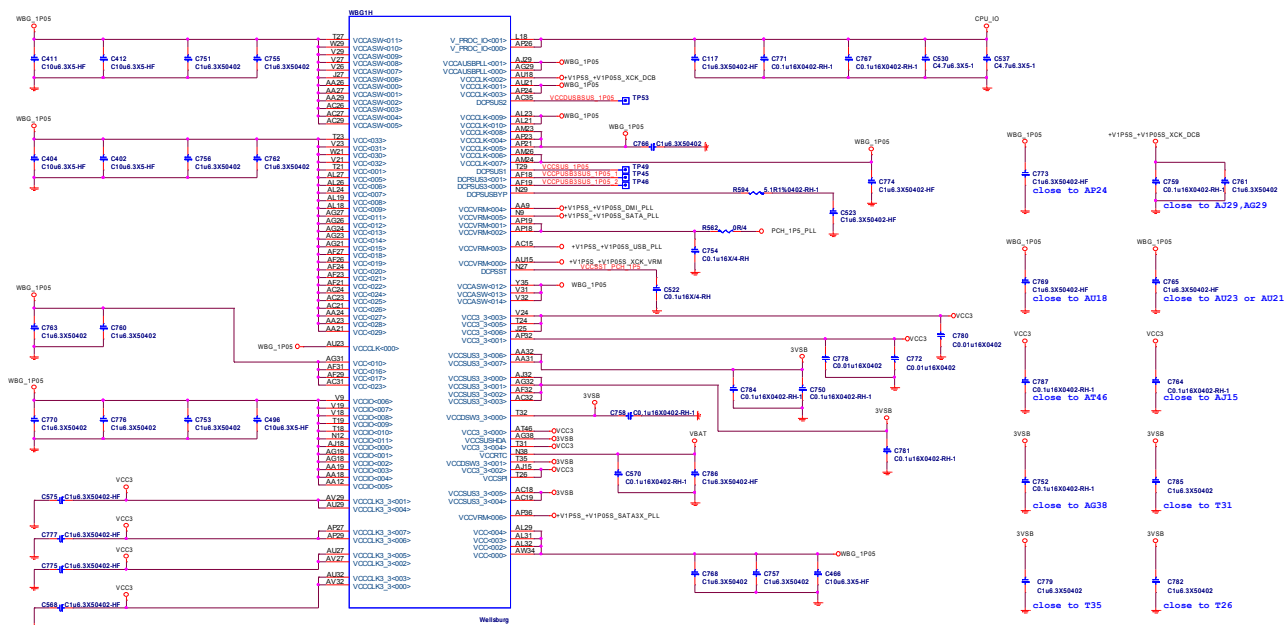
1-2 Clear CMOS  
2-3 Normal



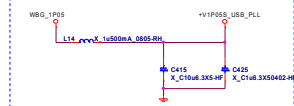


 <b>MSI</b> <small>MICRO-START INT'L CO., LTD.</small> <i>Link to the Future</i>		
<b>MICRO-START INT'L CO.,LTD.</b>		
Title		
<b>WBG-NVRM</b>		
Size	Document Number	Rev
	<b>Centauri</b>	<b>A00</b>
Date	Friday, June 06, 2014	Sheet 23 of 50

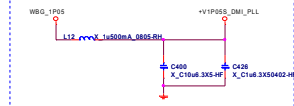
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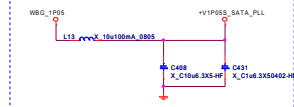
PCB\_USB\_PLL (A215)



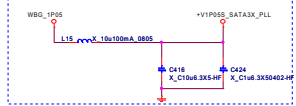
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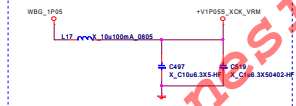
PCB\_SATA3\_PLL (A215)



PCB\_SATA3\_PLL (A215)



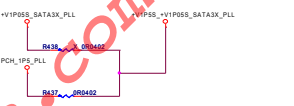
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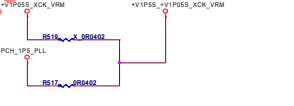
PCB\_SATA3\_PLL (A215)



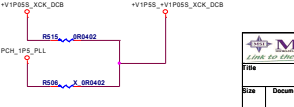
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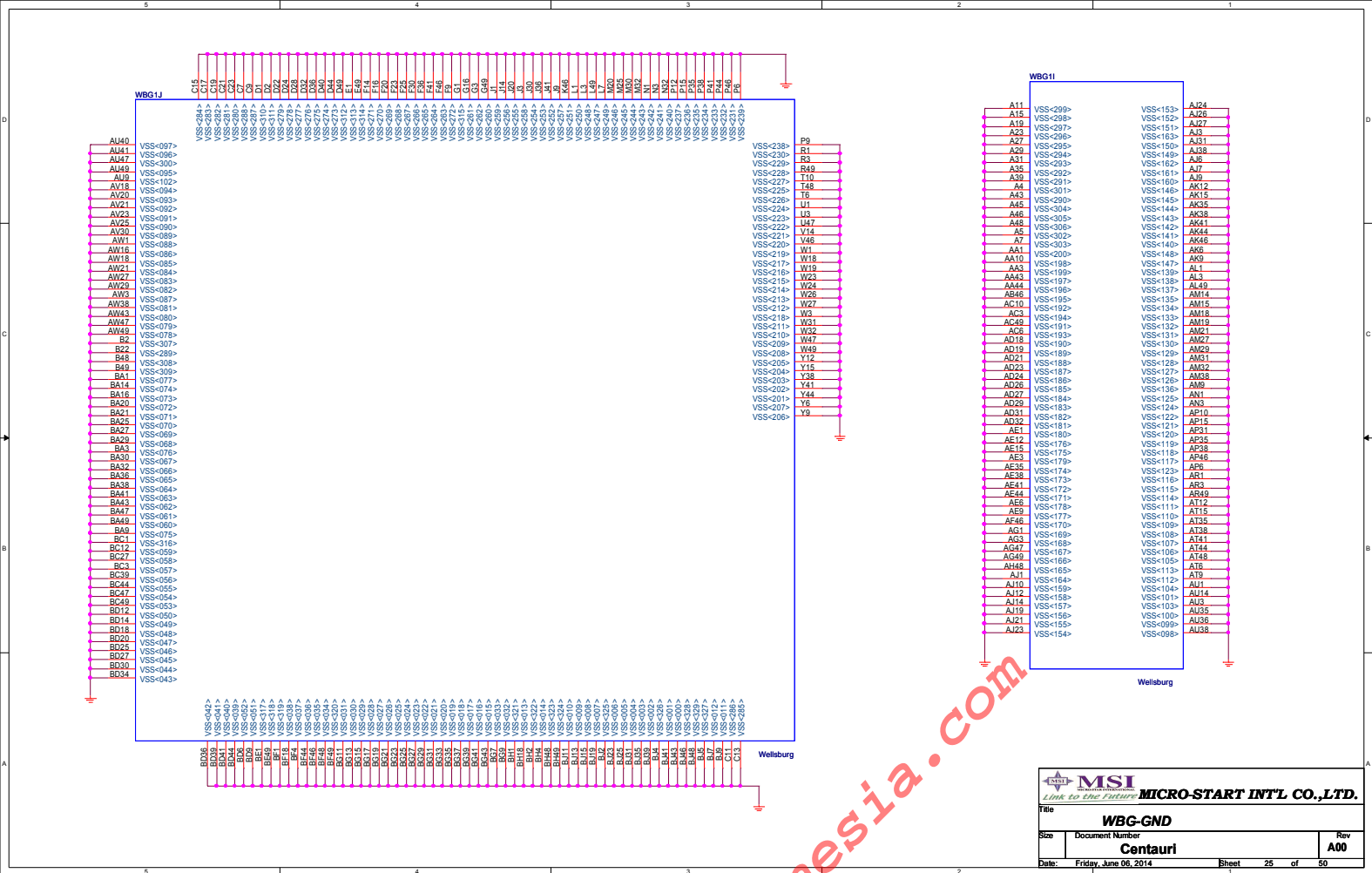
PCB\_DM1\_PLL (A215)



PCB\_SATA3\_PLL (A215)









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4

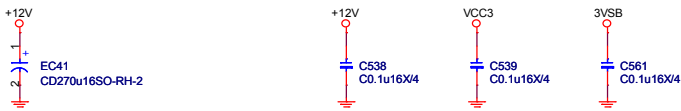
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2

File

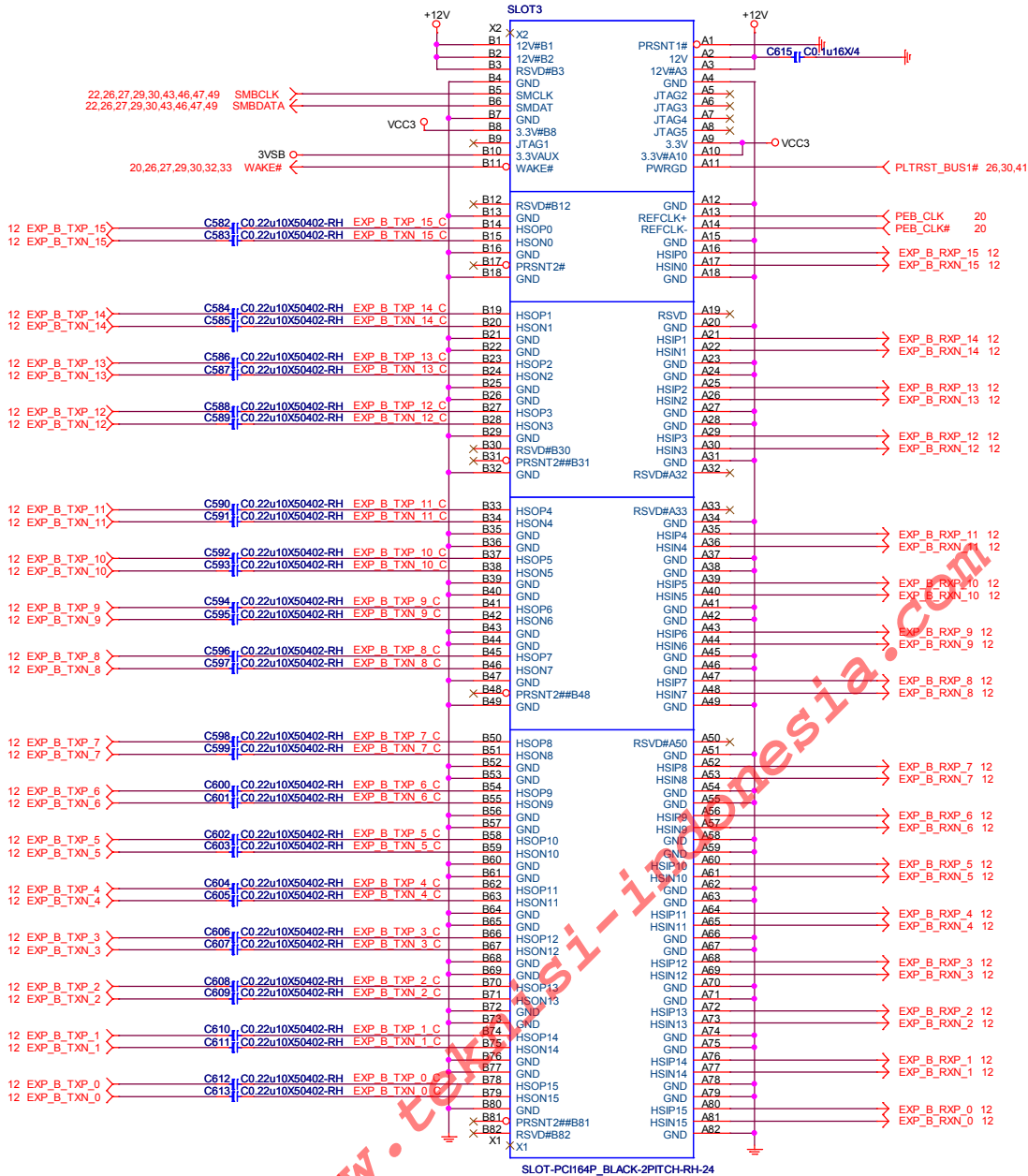
Size Document

Date Friday



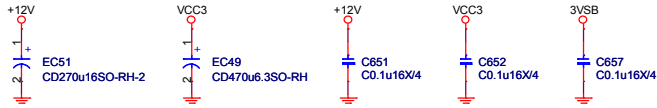
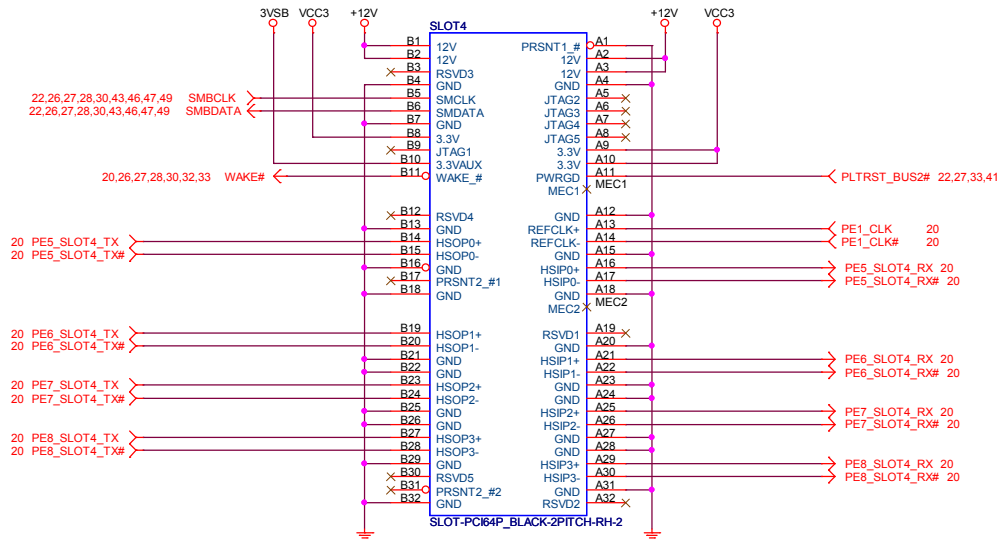
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<b>PCIE X1 Slot2</b>							
<b>Size</b>		<b>Document Number</b>				<b>Rev</b>	
<b>Date</b>		<b>Centauri</b>				<b>A00</b>	
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# PCI EXPRESS X16 SLOT



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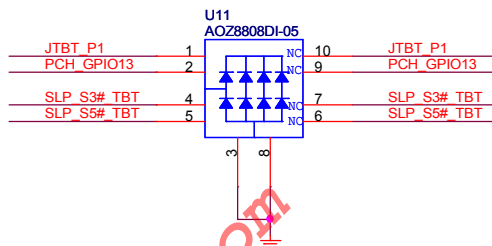
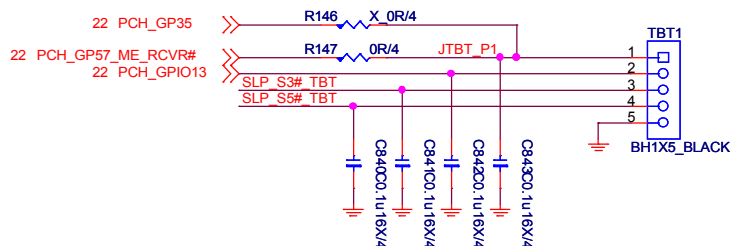
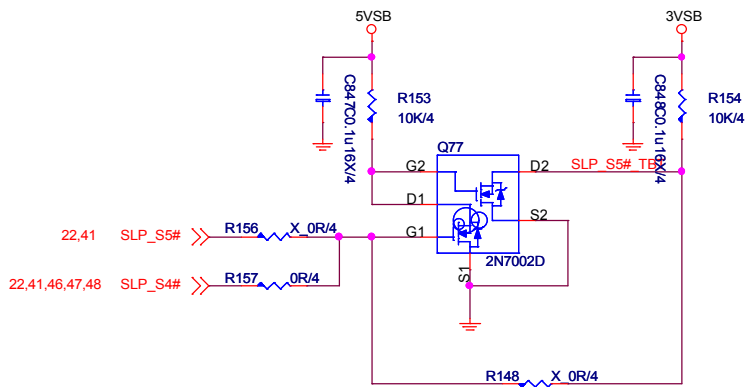
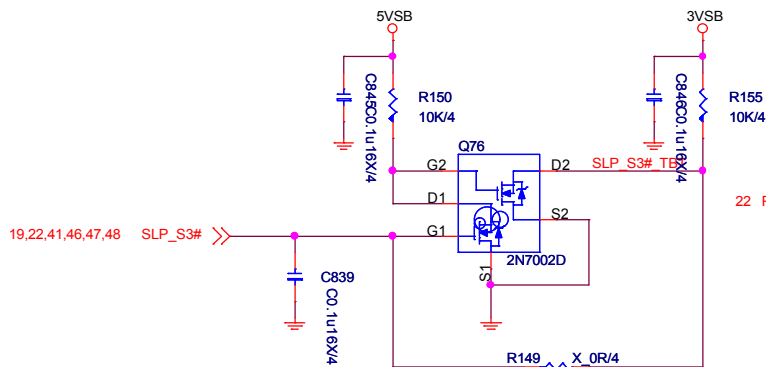
# PCI EXPRESS X4 SLOT




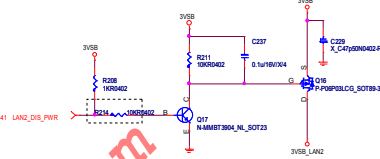
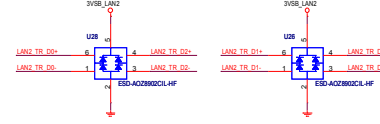
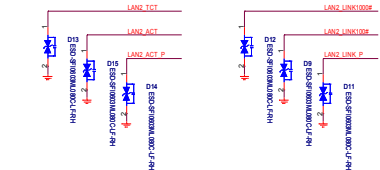
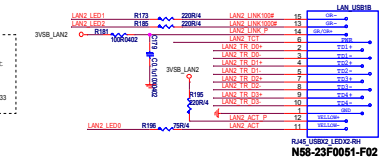
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Title		
<b>PCIE X4 slot4</b>		
Size	Document Number	Rev
	<b>Centauri</b>	<b>A00</b>
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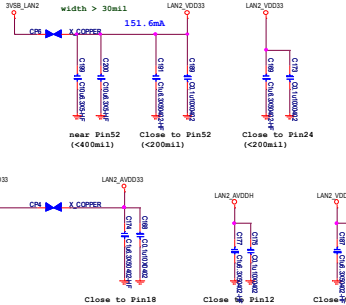
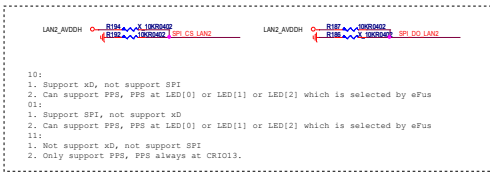





 <b>MSI</b> <small>MICRO-STAR INTERNATIONAL</small> <i>Link to the Future</i>		<b>MICRO-START INT'L CO.,LTD.</b>	
Title			
<b>TBT header</b>			
Size	Document Number		Rev
	<b>Centauri</b>		<b>A00</b>
Date:	Friday, June 06, 2014	Sheet	31 of 50

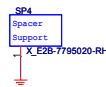
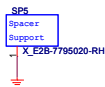
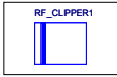
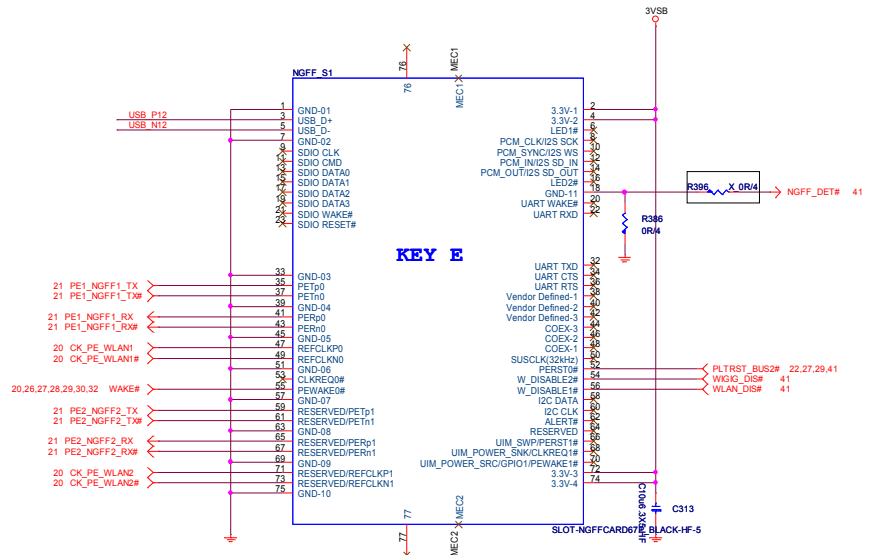
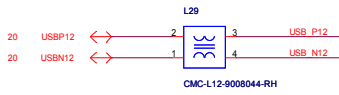


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VDD33 power trace should be wider than 30mils;  
AVDD33 power trace should be wider than 30mils;  
VDD IO power trace should be wider than 30mils;  
VDDIO_REG power trace should be wider than 20mils;  
AVDDH power trace should be wider than 20mils;  
AVDDL power traces should be wider than 20mils.  
DVDDL power traces should be wider than 20mils.
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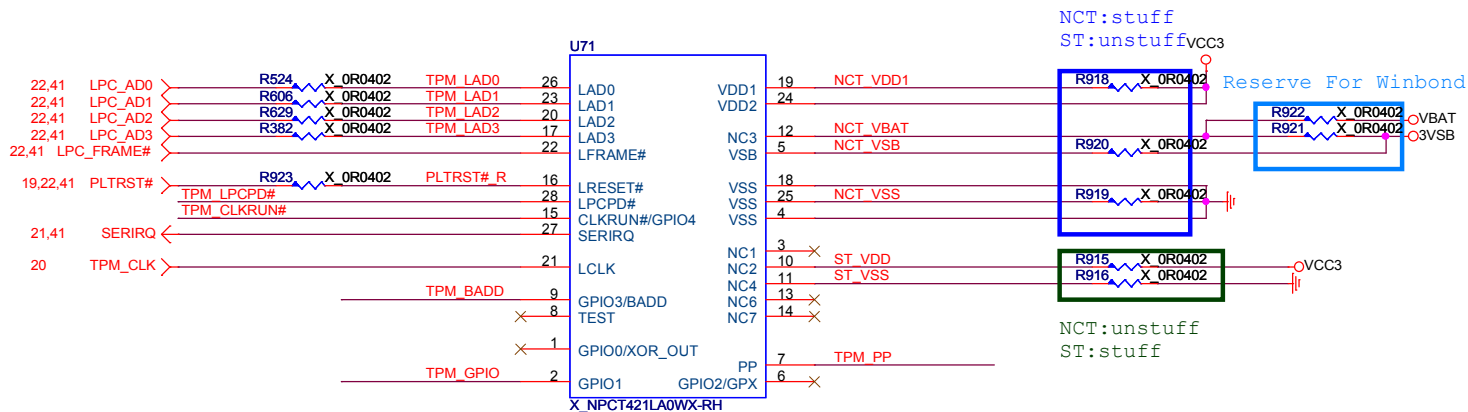
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<b>Size</b>	<b>Document Number</b> <b>Centauri</b>		<b>Rev</b> <b>A00</b>
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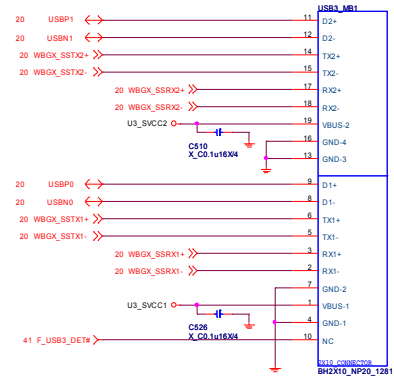
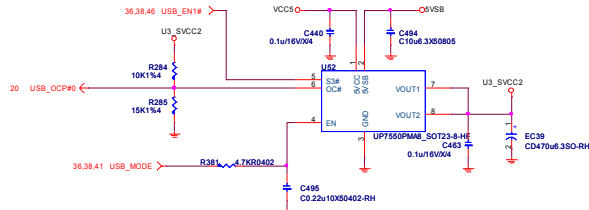
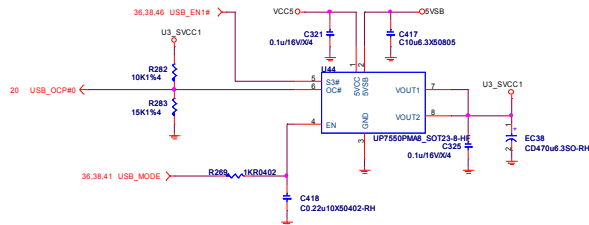
<b>MICRO-START INT'L CO.,LTD.</b>	
<b>NGFF Key E (WLAN)</b>	
Size	Document Number
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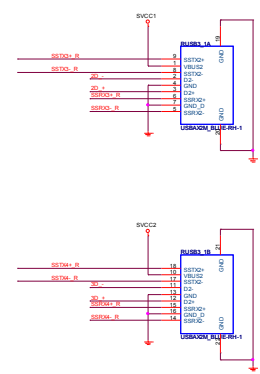
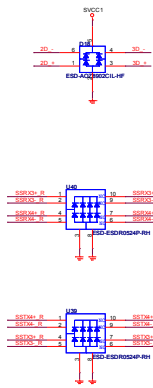
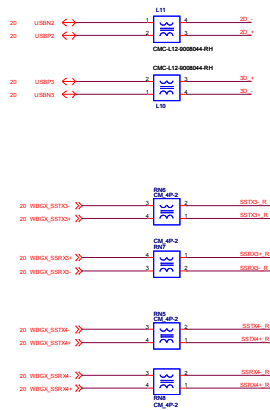
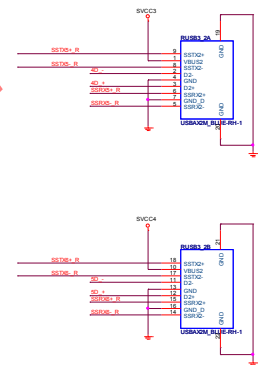
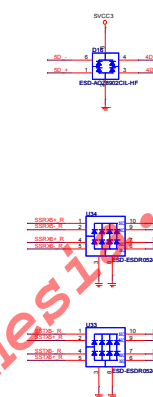
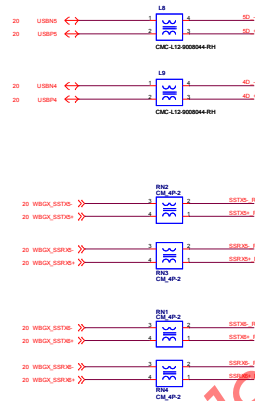
<b>MSI</b> <small>MICRO-STAR INTERNATIONAL</small> <i>Link to the Future</i>		
<b>MICRO-STAR INT'L CO.,LTD.</b>		
Title		
<b>TPM(reserved)</b>		
Size	Document Number	Rev
	<b>Centauri</b>	<b>A00</b>
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# Front USB3.0 Port

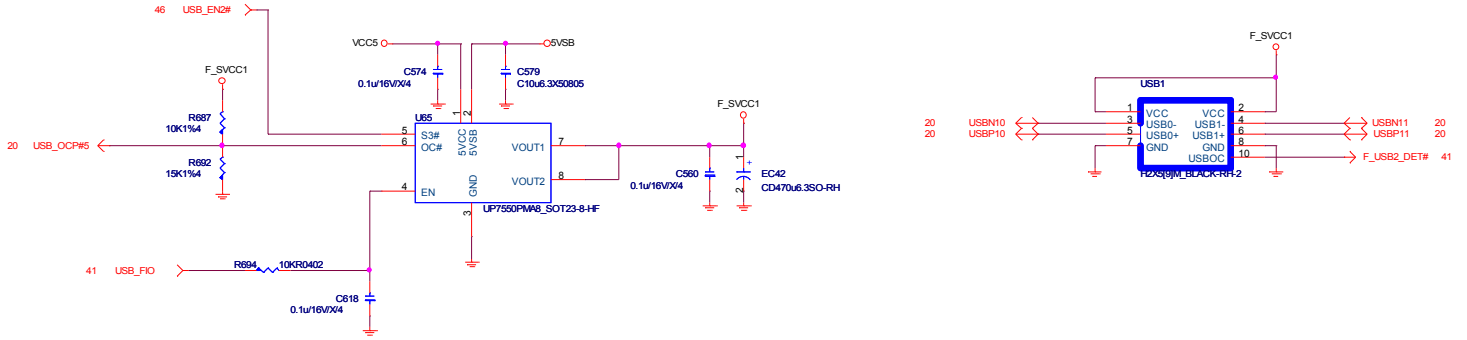


MSI Link to the Future			
MICRO-START INTL CO., LTD.			
File			
Front USB3.0			
Size			
Document Number			
Centauri			
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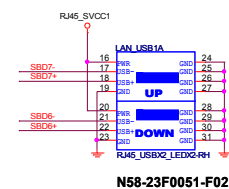
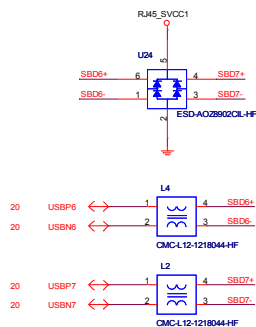
[illegible]

# **Front USB2.0 Port 11/12**

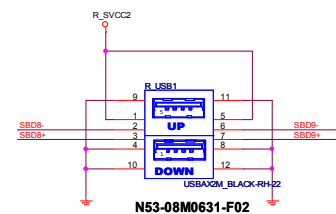
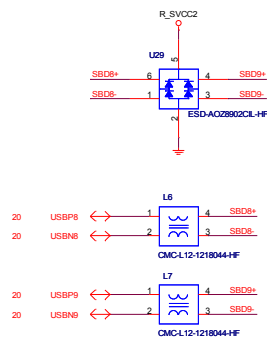


<div> <div> <div>MSI</div> <div>Link to the Future</div> </div> <div>MICRO-START INTL CO.,LTD.</div> </div>			
Title			
Front USB2.0 x2			
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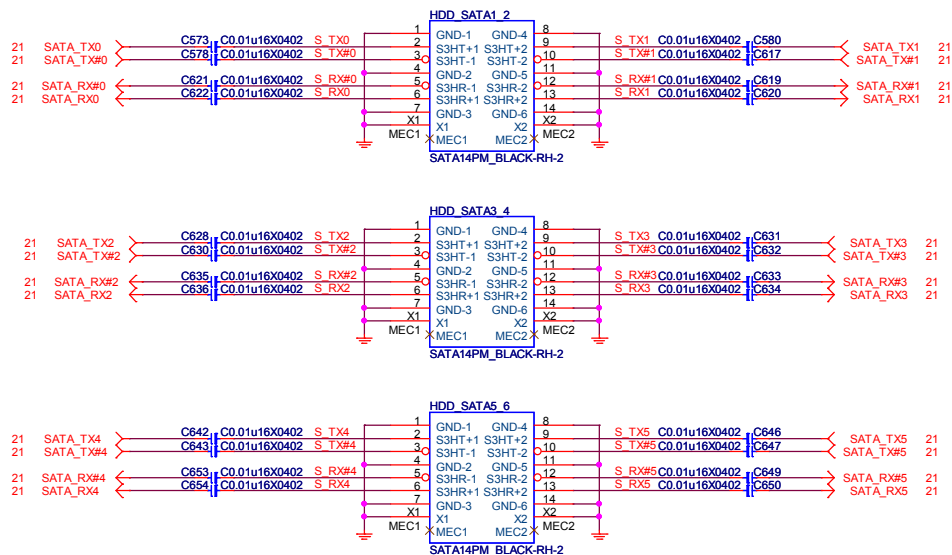
### Rear USB2.0 Port 7 / 8




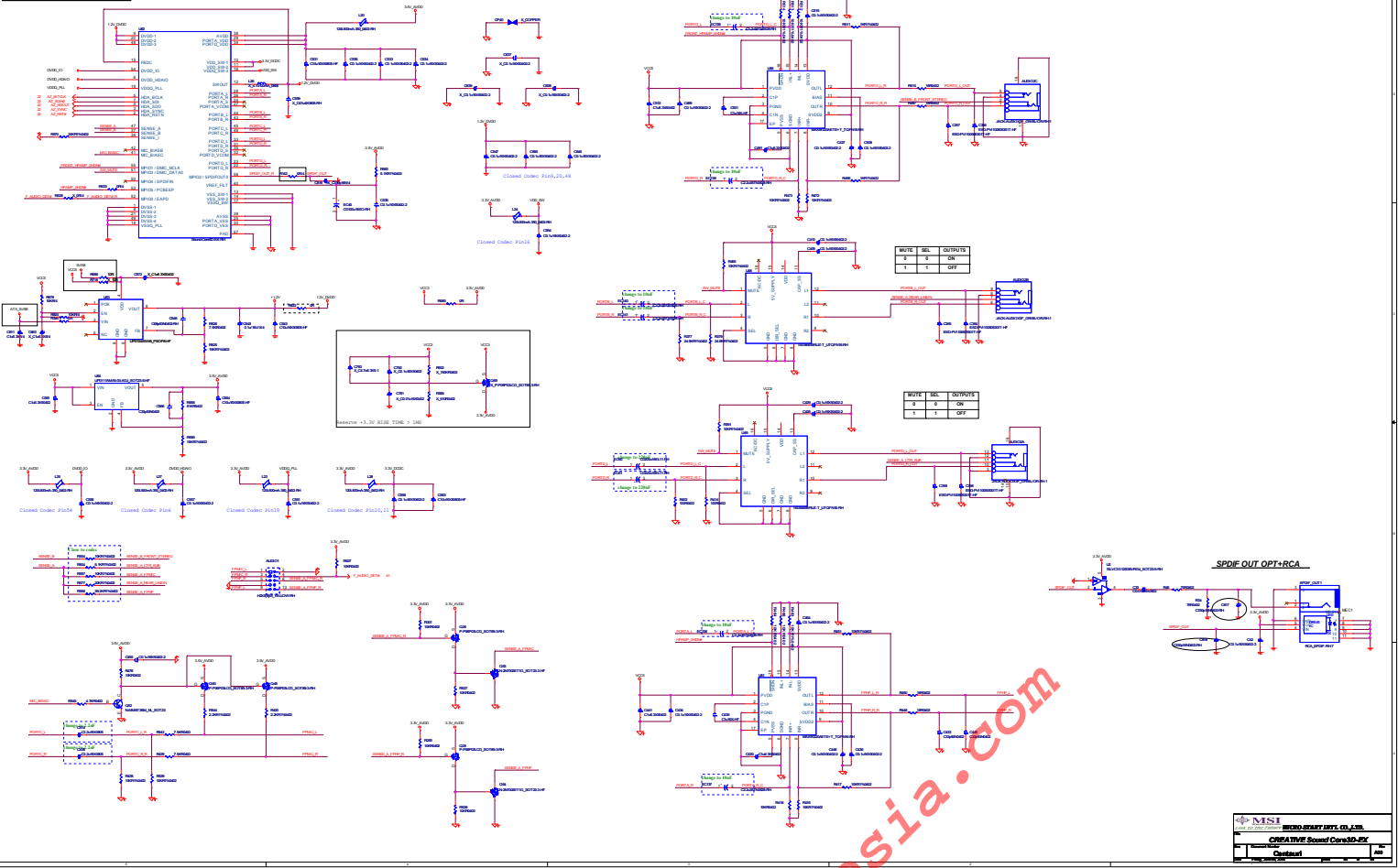
### Rear USB2.0 Port 9 / 10



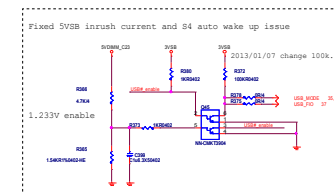
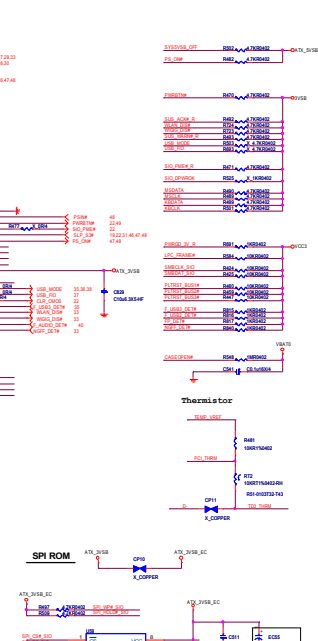
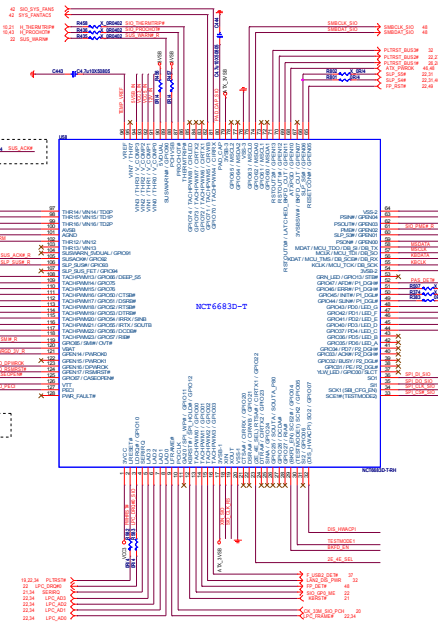
# SATA 3.0 Connector



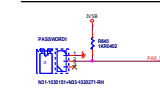
 <b>MSI</b> <small>Link to the Future</small>		<b>MICRO-START INT'L CO.,LTD.</b>	
<b>Title</b> <b>SATA PORT</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b> <b>A00</b>
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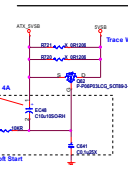




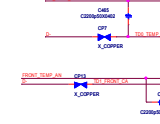
### PASSWORD DETECTION



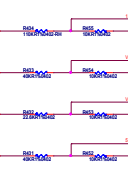
### 5VSB Power Switch



### Place close to VBM MOSFET



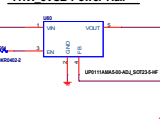
### Voltage Sensing



### Power On Strapping Table

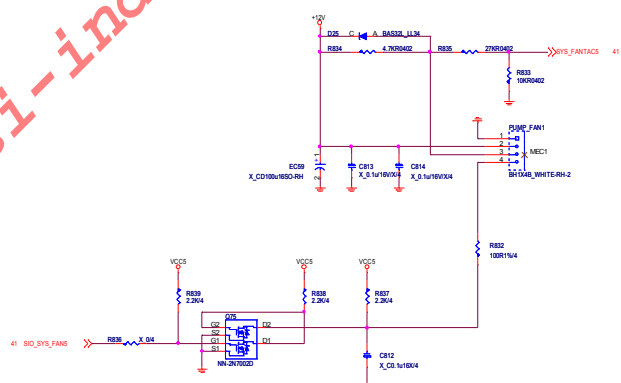
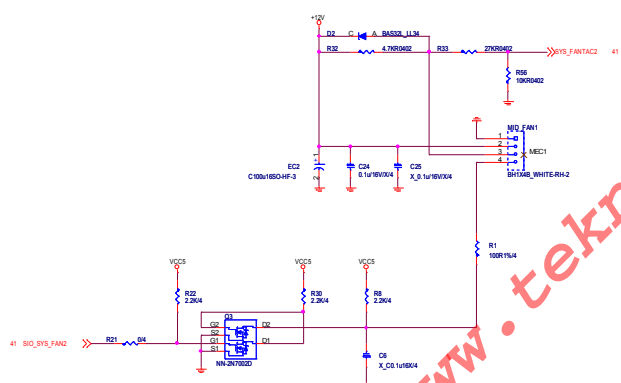
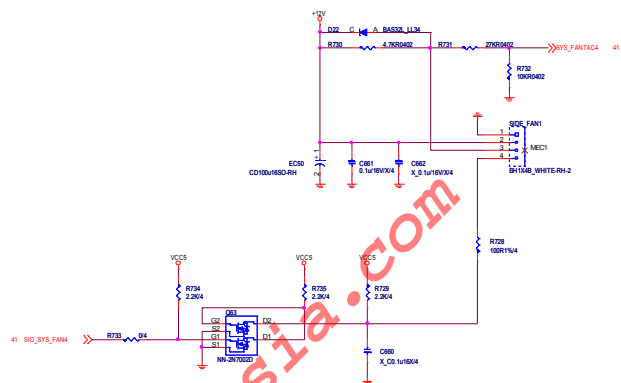
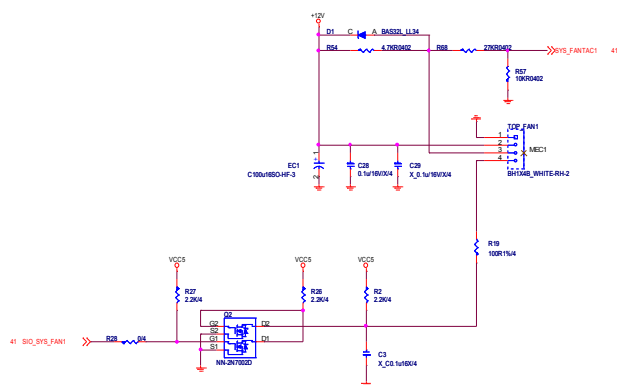
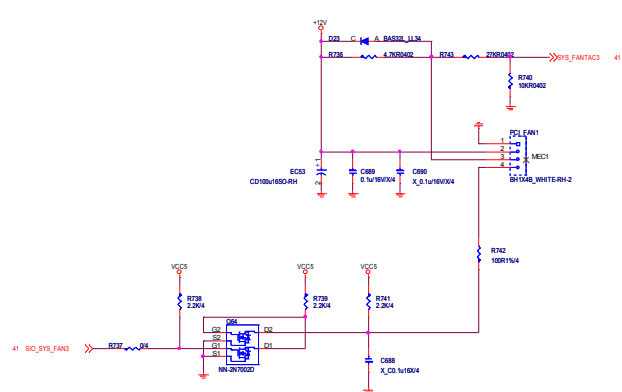
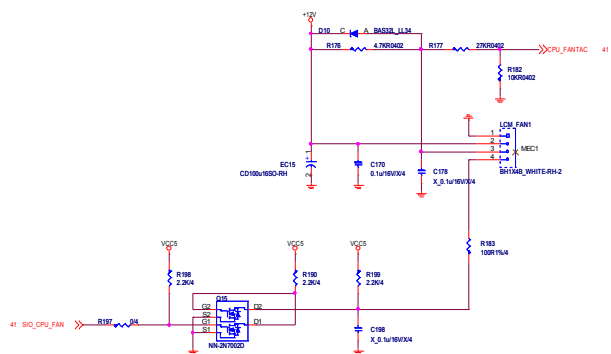
Symbol	Value	Description
SE_4E_SEL	0	SIO I/O address is 4E20F0
BAFD_EN	1	PMU7 BIOS/BIOS Pin# RSTOUTEN
YESMODE1	1	PMU7 BIOS/BIOS Pin# LATCHES_BIOS_OUT
DIS_WRAOP	0	Hardware ACPI could take over related signals
DIS_WRAOP	1	Hardware ACPI never take over related signals
RESMODE2	0	Configuration Register I/O port is 4E4F
RESMODE2	1	Configuration Register I/O port is 4E4F
RES_CPS_SEL	0	Switches open or close are determined by ATSPD0
RES_CPS_SEL	1	Switches open or close are determined by configuration register

### ATX 3VSB Power Rail

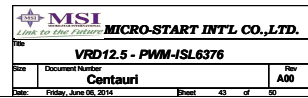


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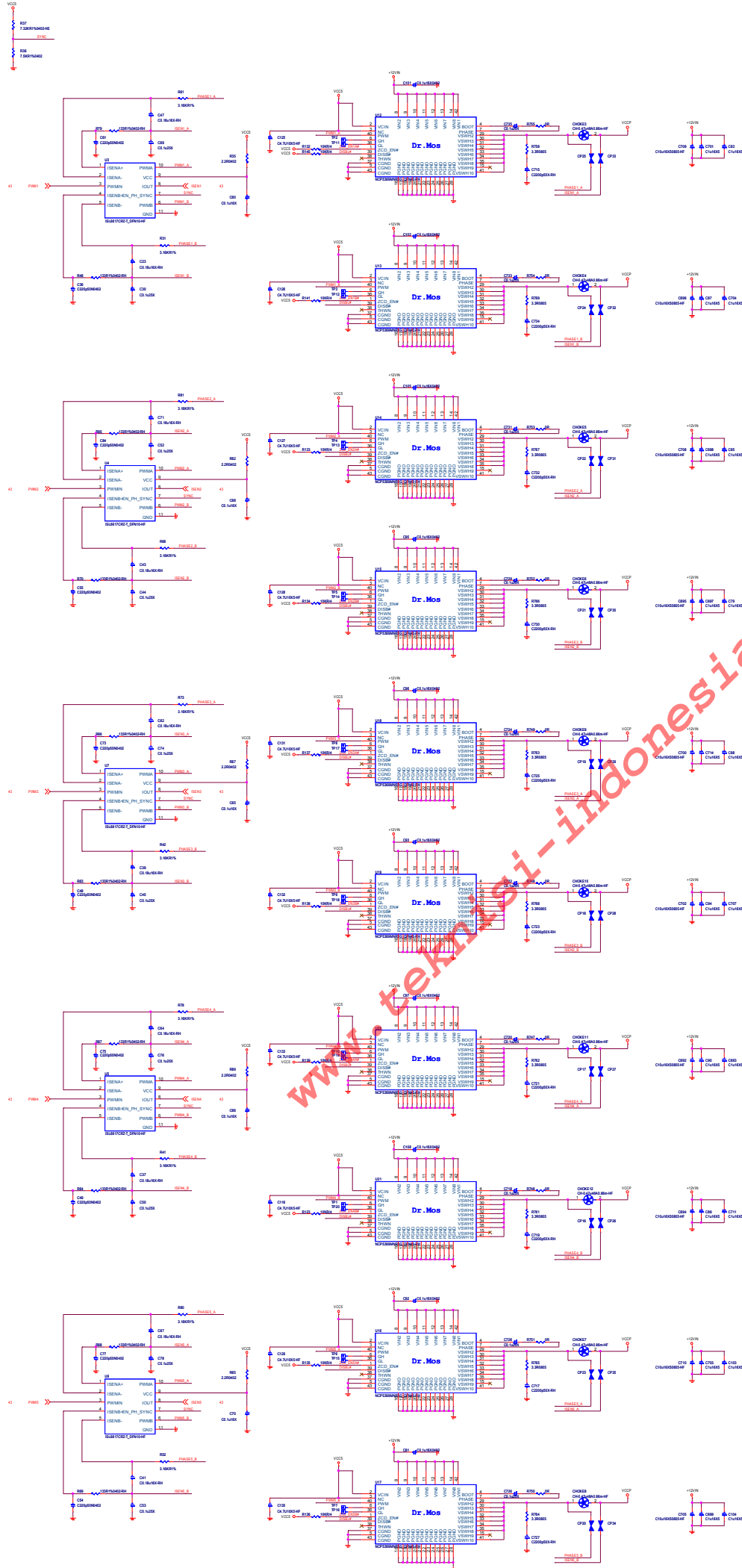
CPU Fan



close to VRM



Pin descriptions	Rup	Rdown	Registers
BTS_DES_TCOMPS	499K	NC	DFh
BT_FVID_TCOMP	499K	NC	DFh
ADDR_IMAXS_TMAX	NC	10K	0h
NPSI_DE_IMAX	845K	267K	63h



VCCP

C261 00001 FH

C262 00001 FH

C263 00001 FH

C264 00001 FH

C265 00001 FH

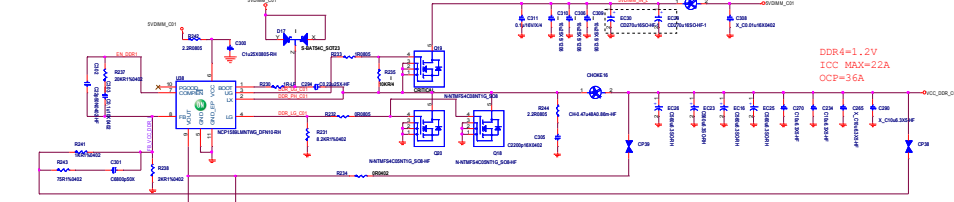
C266 00001 FH

C267 00001 FH

C268 00001 FH

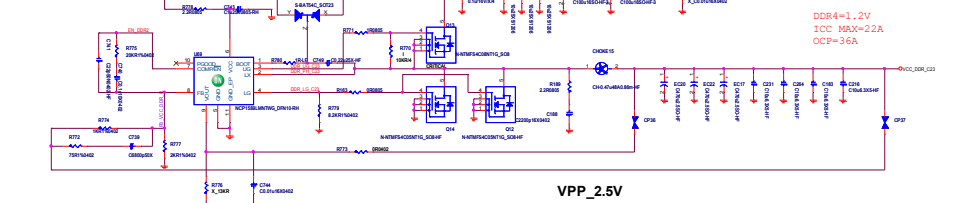
DDR III 1.2V POWER

Switch 1 Phase 1.2V 33A

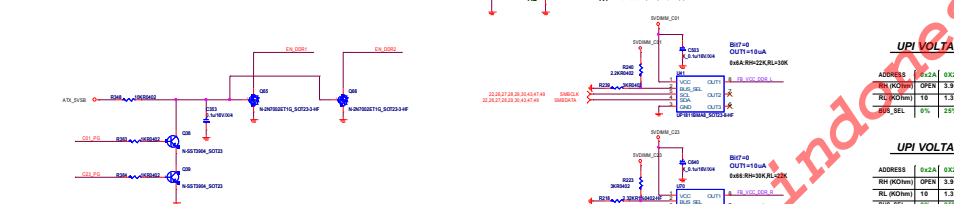
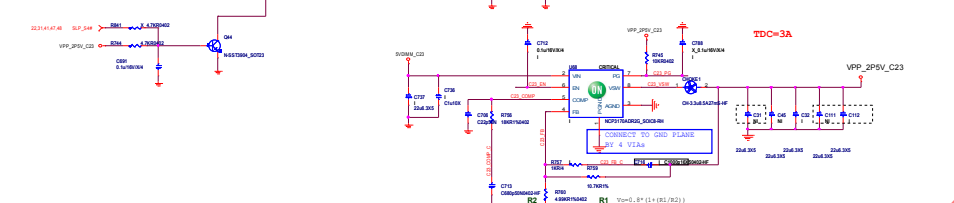
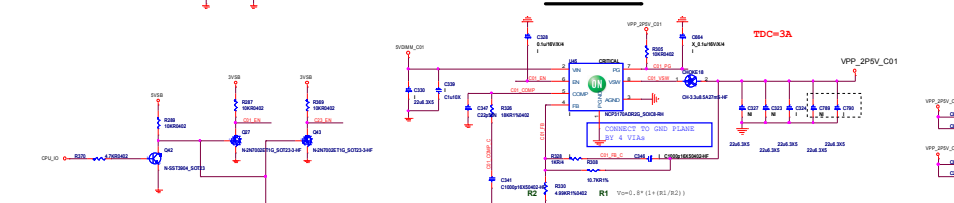


DDR III 1.2V POWER

Switch 1 Phase 1.2V 33A

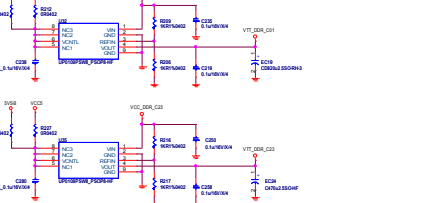


VPP\_2.5V

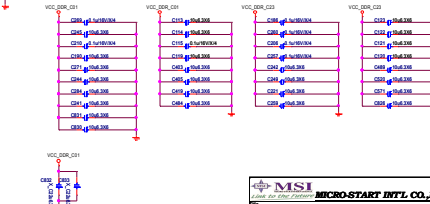
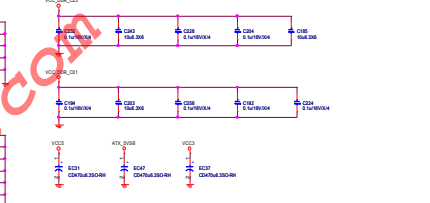
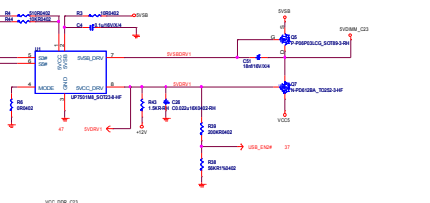
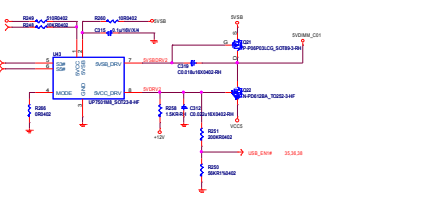


DDR4 Termination Power

VTT=1/2 VDDQ



DDR4 Regulator Power Source



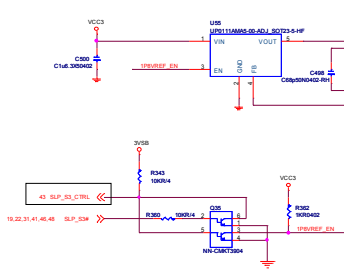
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x2B	0x2C	0x2D	0x2E
REL_VOLTAGE	1.8	1.3	2.3	1	3.9
BUR_SEL	0%	25%	40%	60%	100%

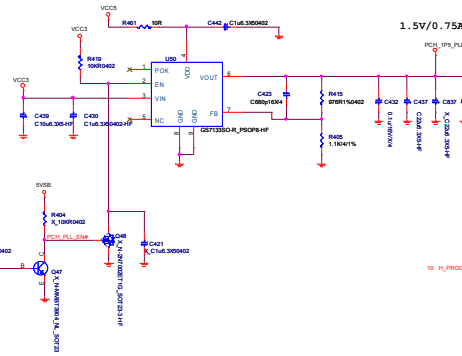
UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x2B	0x2C	0x2D	0x2E
REL_VOLTAGE	1.8	1.3	2.3	1	3.9
BUR_SEL	0%	25%	40%	60%	100%

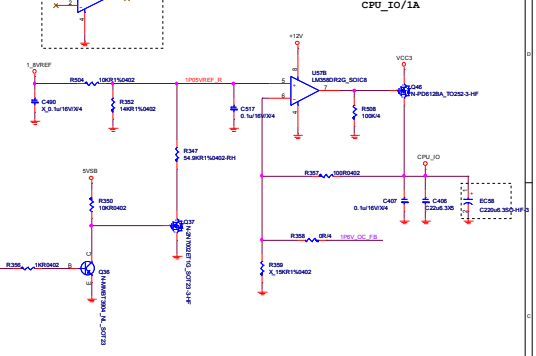
### 1.8V Reference Power



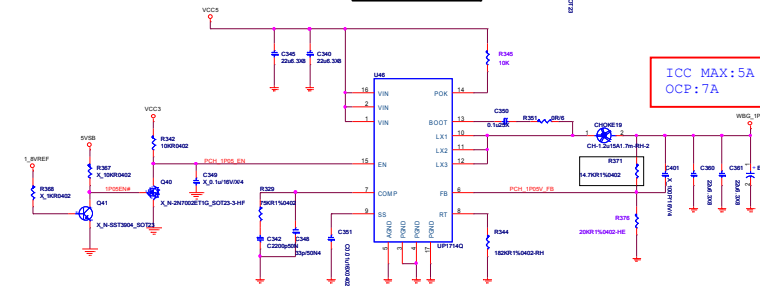
### WBG 1.5V PLL Power Rail



### CPU IO 1.05V Power Rail



### PCH Core Power

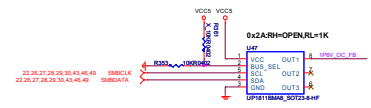


$$R2 = R1 / [(Vout / 0.6V) - 1]$$

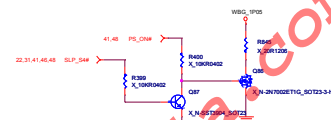
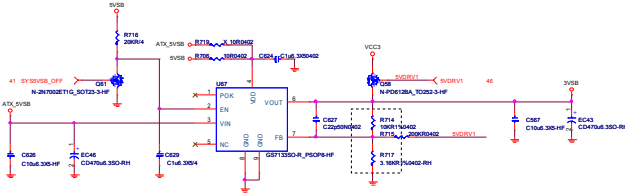
PROC_ID	VOUT
0	0.95V
1	1.05V

### UPI VOLTAGE CONSOLE

ADDRESS	0x2A	0x2B	0x2C	0x2D	0x2E
0	0x2A	0x2B	0x2C	0x2D	0x2E
1	0x2A	0x2B	0x2C	0x2D	0x2E
BUS_SEL	95%	25%	40%	60%	75%

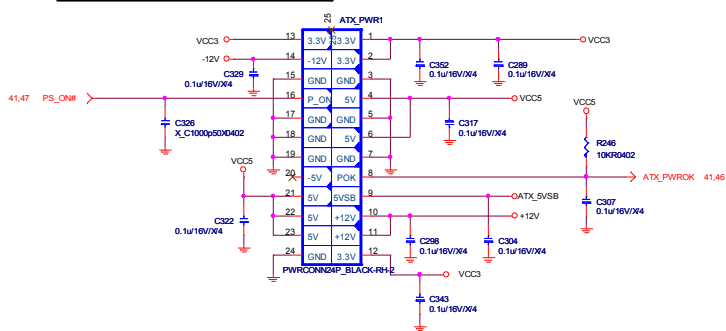


### 3VSB Power Rail

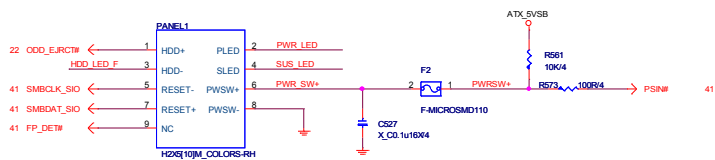


MSI MICRO-START INTL CO., LTD.	
PCH Core Power	
Doc No.	Centauri
Rev.	A00

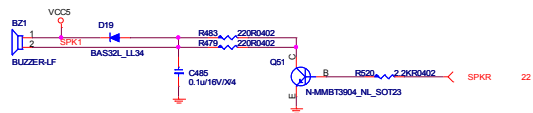
## 24 Pin ATX Power Connector



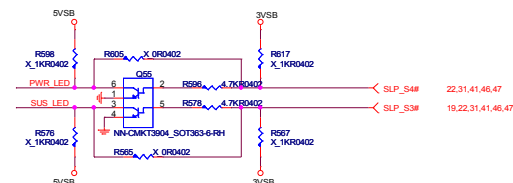
## Front Panel



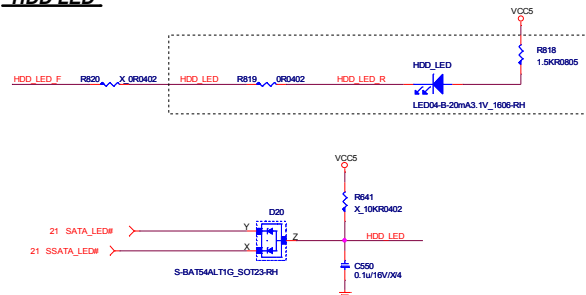
## Buzzer Circuit



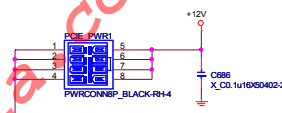
## Power LED



## HDD LED



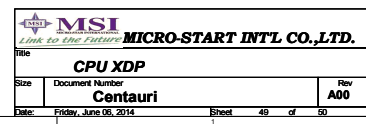
## GFX Power



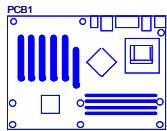
MSI			
Link to the Future			
MICRO-START INT'L CO.,LTD.			
Title			
ATX/F Panel/LED			
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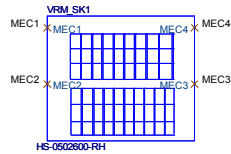
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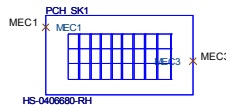
## Manual Parts



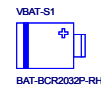
PF0-0786210-ZX4



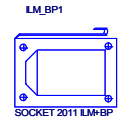
HS-0502600-RH



HS-0406680-RH



BAT-BCR2032P-RH

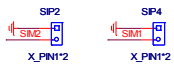


SOCKET 2011 ILM-BP

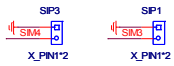
## Simulation



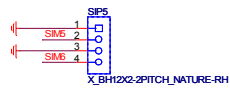
BIOS-STICKER



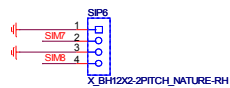
X\_PIN1\*2



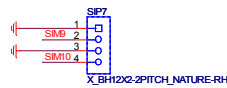
X\_PIN1\*2



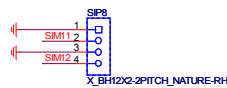
X\_BH12X2-2PITCH\_NATURE-RH



X\_BH12X2-2PITCH\_NATURE-RH



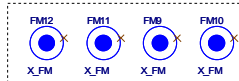
X\_BH12X2-2PITCH\_NATURE-RH



X\_BH12X2-2PITCH\_NATURE-RH

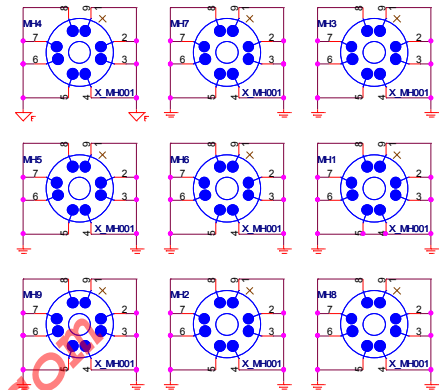
## Optics Orientation Holes



### Optical Fiducial Marks-120



## PCB Mounting Holes

### Mounting Holes



  <b>MICRO-START INTL CO.,LTD.</b> <i>Link to the Future</i>			
<b>Title</b>			
<b>Manual Parts Parts</b>			
<b>Size</b>	<b>Document Number</b>		<b>Rev</b>
	<b>Centauri</b>		<b>A00</b>
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